AKTU

GATEWAY CLASSES

Digital System Design

B.Tech. 3rd Sem

EC & Allied



Exam/Result Oriented Content

- ✓ Recorded Video Lectures
- ✓ Pdf Notes
- ✓ PYQs

DIGITAL SYSTEM DESIGN

UNIT 4 : Logic families and semiconductor memories

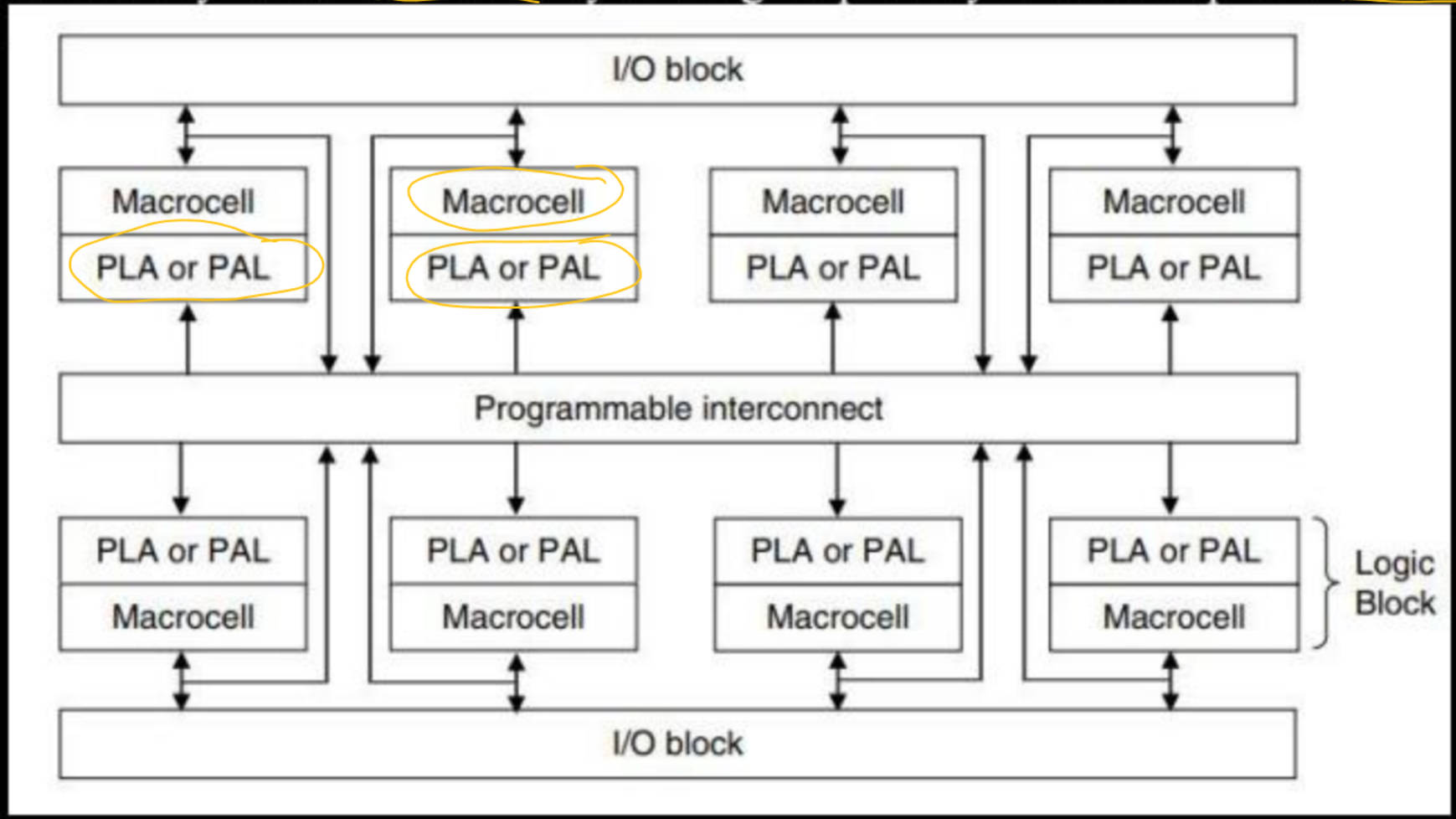
Lec 7

Today's Target

- Complex Programmable Logic Devices
- FPGA
- Components of an FPGA
- FPGA Programming Technologies

Complex Programmable Logic Devices (CPLDs)

- It is developed on top of PLD devices to create much larger and complex designs.
- A CPLD consists of a number logic blocks (or functional blocks), which internally consists of either a PLA or a PAL along with a Macrocell.
- Macrocell consists of any additional circuitry and signal polarity control to provide true signal or its complement.

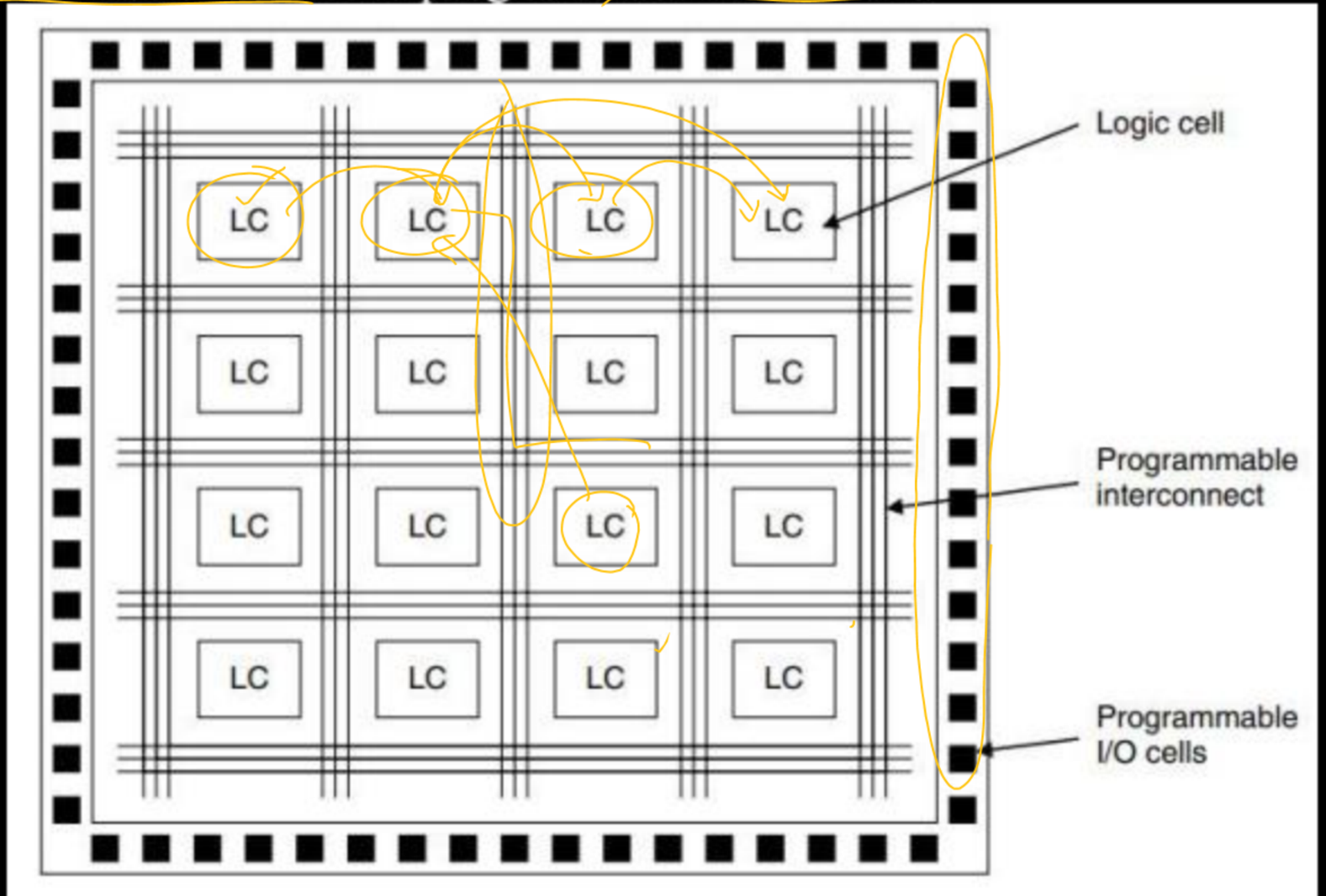


What is an FPGA?

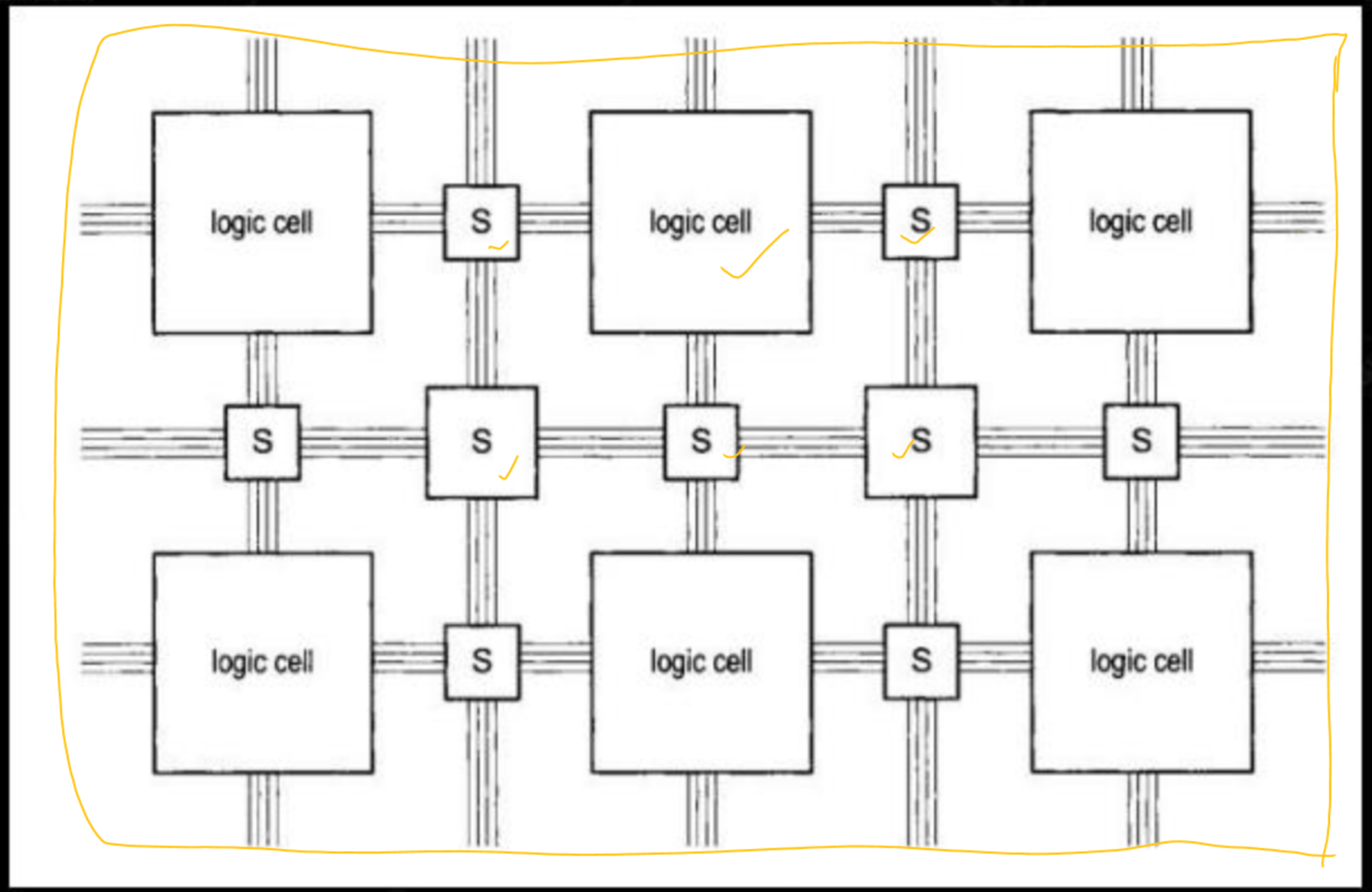
- Field Programmable Gate Arrays or FPGAs in short are pre-fabricated Silicon devices that consists of a matrix of reconfigurable logic circuitry and programmable interconnects arranged in a two-dimensional array.
- The programmable Logic Cells can be configured to perform any digital function and the programmable interconnects (or switches) provide the connections among different logic cells.
- Using an FPGA, you can implement any custom design by specifying the logic or function of each logic block and setting the connection of each programmable switch.
- Since this process of designing a custom circuit is done in the field rather than in a fab, the device is known as “Field Programmable”.

Field Programmable Gate Arrays (FPGA)

- FPGA are even more complex than CPLDs.
- The architecture of an FPGA is completely different as it consists of programmable Logic Cells, programmable interconnects and programmable IO blocks.



Internal Structure of an FPGA



- The core of the FPGA is made up of configurable logic cells and programmable interconnections.
- These are surrounded by a number of programmable IO blocks, which are used to talk to the external world.

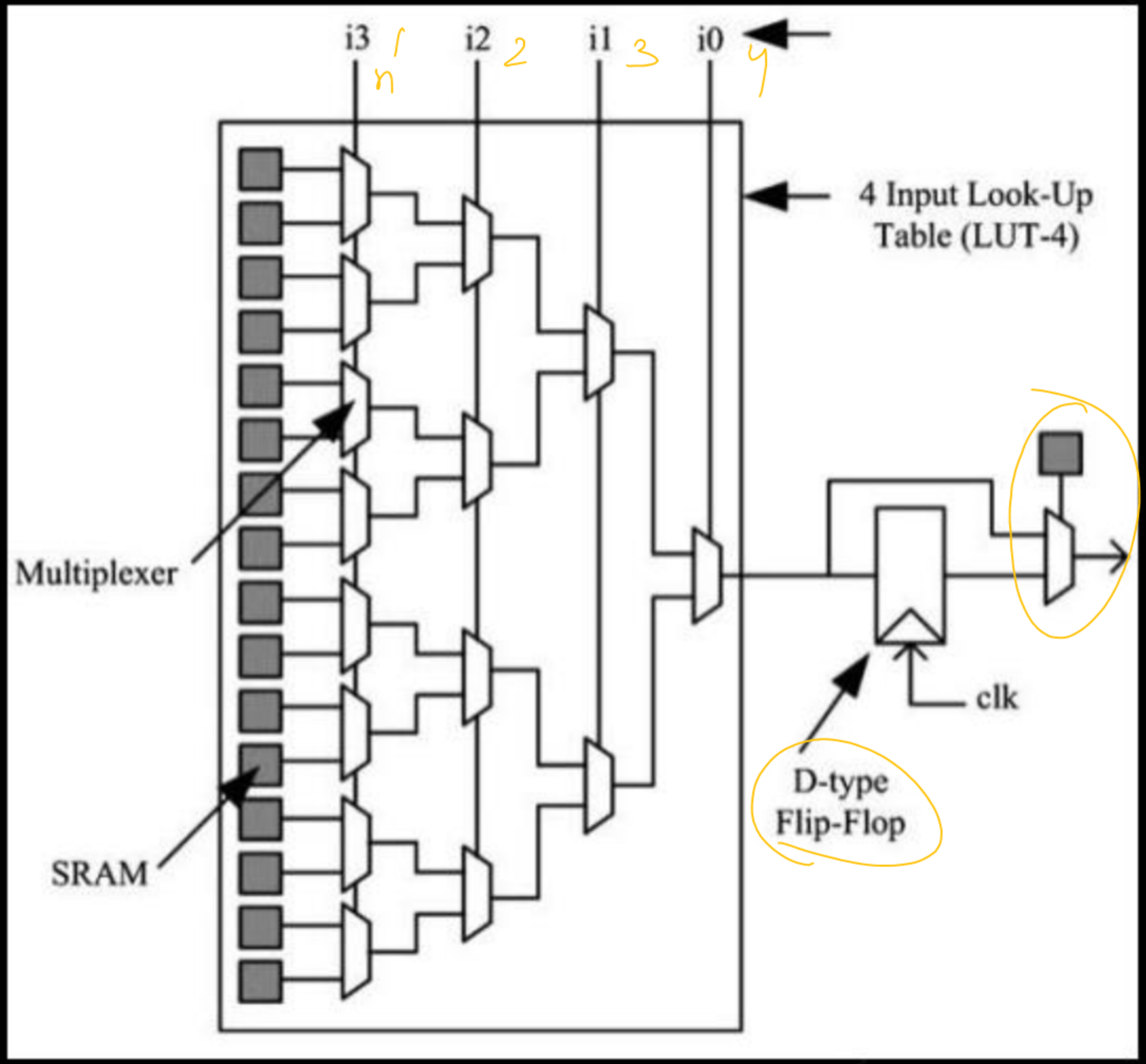
Components of an FPGA

Typically, an FPGA consists of three basic components. They are:

- Programmable Logic Cells (or Logic Blocks) – responsible for implementing the core logic functions.
- Programmable Routing – responsible for connecting the Logic Blocks.
- IO Blocks – which are connected to the Logic Blocks through the routing and help to make external connections.

Logic Block

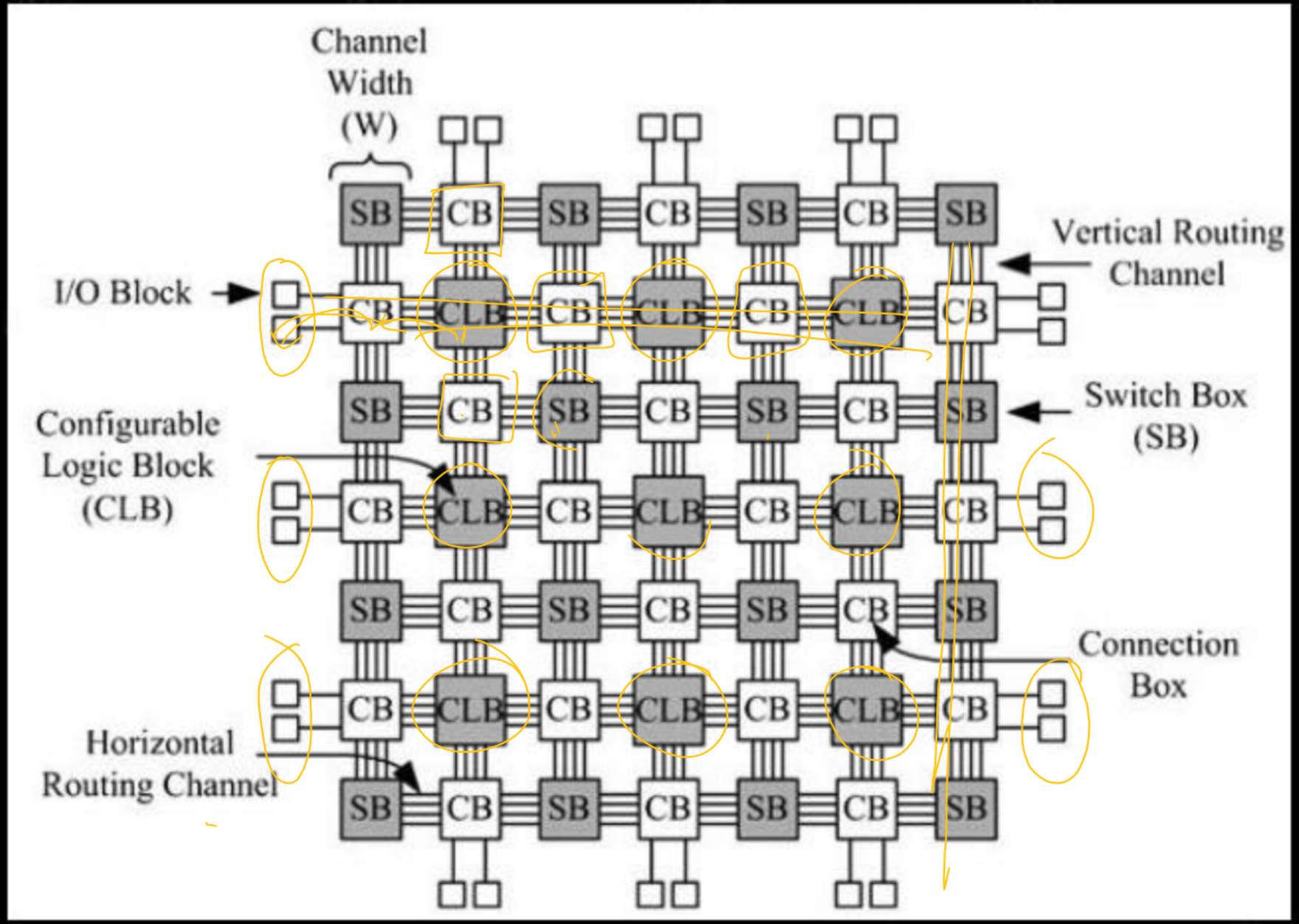
- The Logic Block in Xilinx based FPGAs are called as Configurable Logic Blocks or CLB while the similar structures in Altera based FPGAs called Logic Array Blocks or LAB.
- A CLB is the basic component of an FPGA, which provides both the logic and storage functionalities.
- The basic logic block can be anything like a transistor, a NAND gate, Multiplexers, Look-up Table (LUT), a PAL like structure or even a processor.
- Both Xilinx and Altera use Look-up Table (LUT) based logic blocks to implement the logic as well as the storage functionalities.
- A Logic Block can be made up of a single Basic Logic Element or a set of interconnected Basic Logic Elements, where a Basic Logic Element is a combination of a Look-up table (which is in turn made up of SRAM and Multiplexers) and a Flip-flop.
- A LUT with 'n' inputs consists of 2^n configuration bits, which are implemented by SRAM Cells. Using these 2^n SRAM Bits, the LUT can be configured to implement any logical function.


i3
i2
i1
i0
4 Input Look-Up Table (LUT-4)
Multiplexer
SRAM
D-type Flip-Flop
clk

Routing

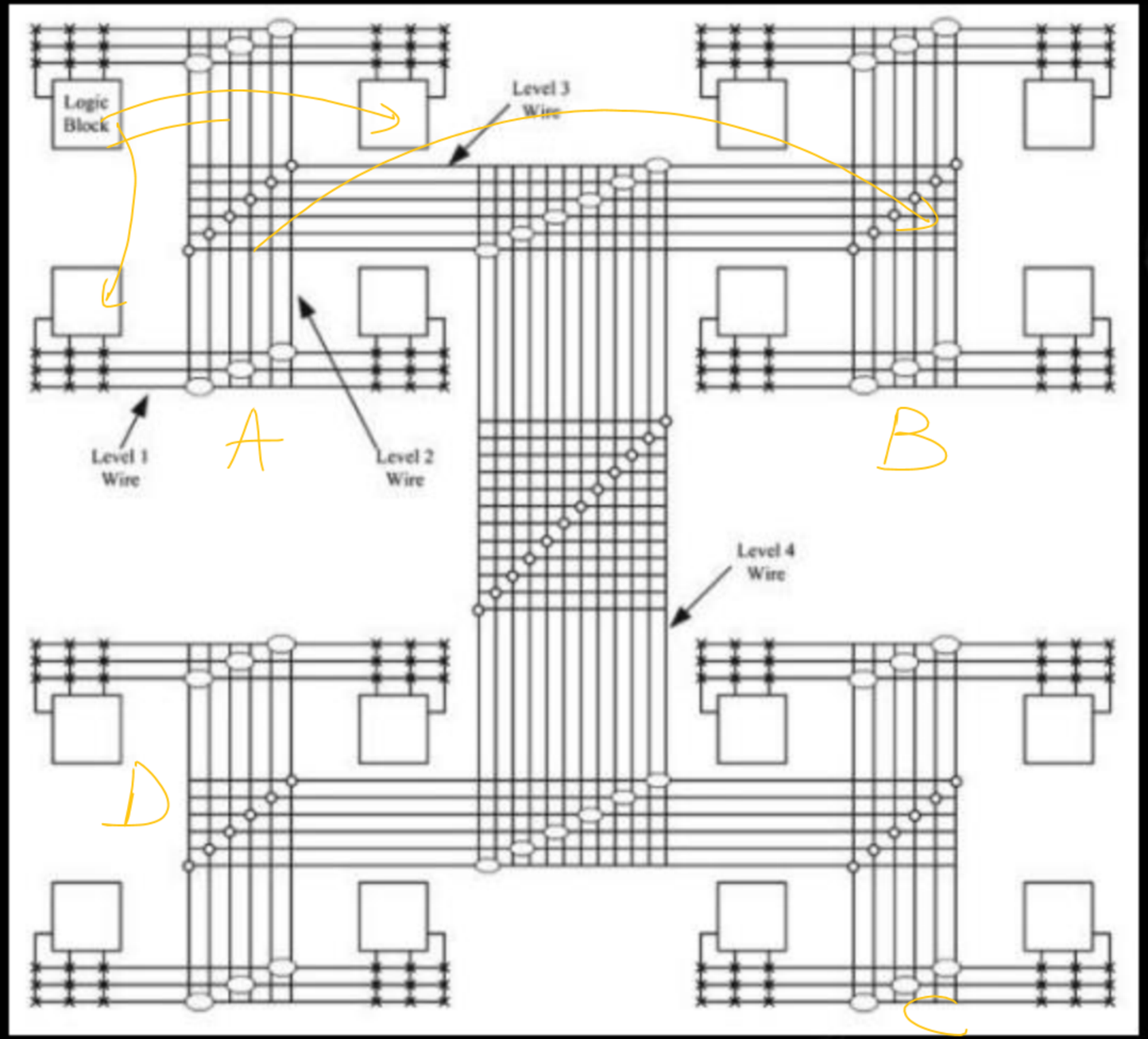
- The programmable routing network is responsible for interconnecting these logic blocks.
- The Routing Network provides interconnections between one logic block to other as well as between the logic block and the IO Block to completely implement a custom circuit.
- Basically, the routing network consists of connecting wires with programmable switches, which can be configured using any of the programming technologies.
- There are basically two types of routing architectures. They are:
- 1) Island Style Routing (also known as Mesh Routing)
- 2) Hierarchical Routing
- In island style routing architecture, the logic blocks are arranged in a two-dimensional array and are interconnected using a programmable routing network.
- This type of routing is widely used in commercial FPGAs.

Island Style Routing



Hierarchical Routing

- Many logic blocks are confined to a local set of connections and hierarchical routing architecture makes use of this feature by dividing the logic blocks into several groups or clusters.
- If the logic blocks are residing in the same cluster, then the hierarchical routing connects them in a low level of hierarchy.
- If the logic blocks are residing in different clusters, then wiring is done over a higher level of hierarchy.


Logic Block
Level 3 Wire
Level 1 Wire
A
Level 2 Wire
B
Level 4 Wire
D
C

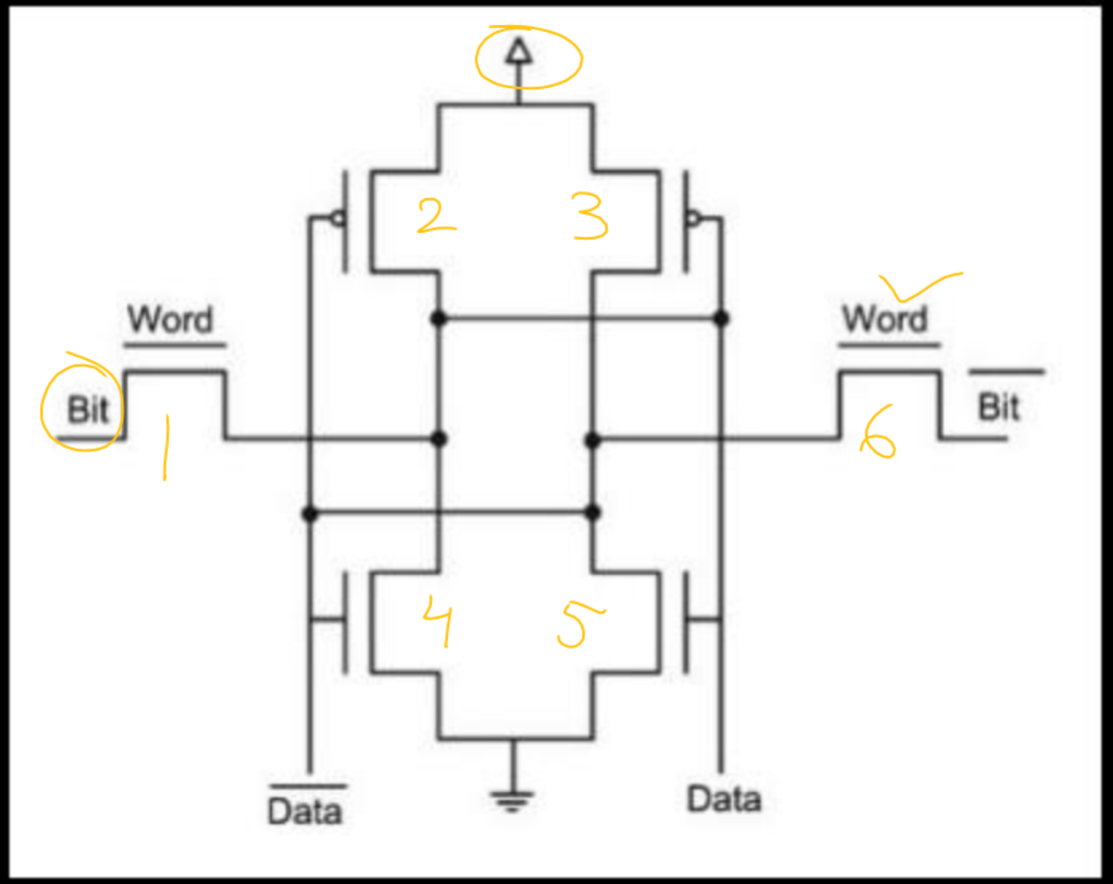
FPGA Programming Technologies

The following are three of the well-known programming technologies used in FPGAs.

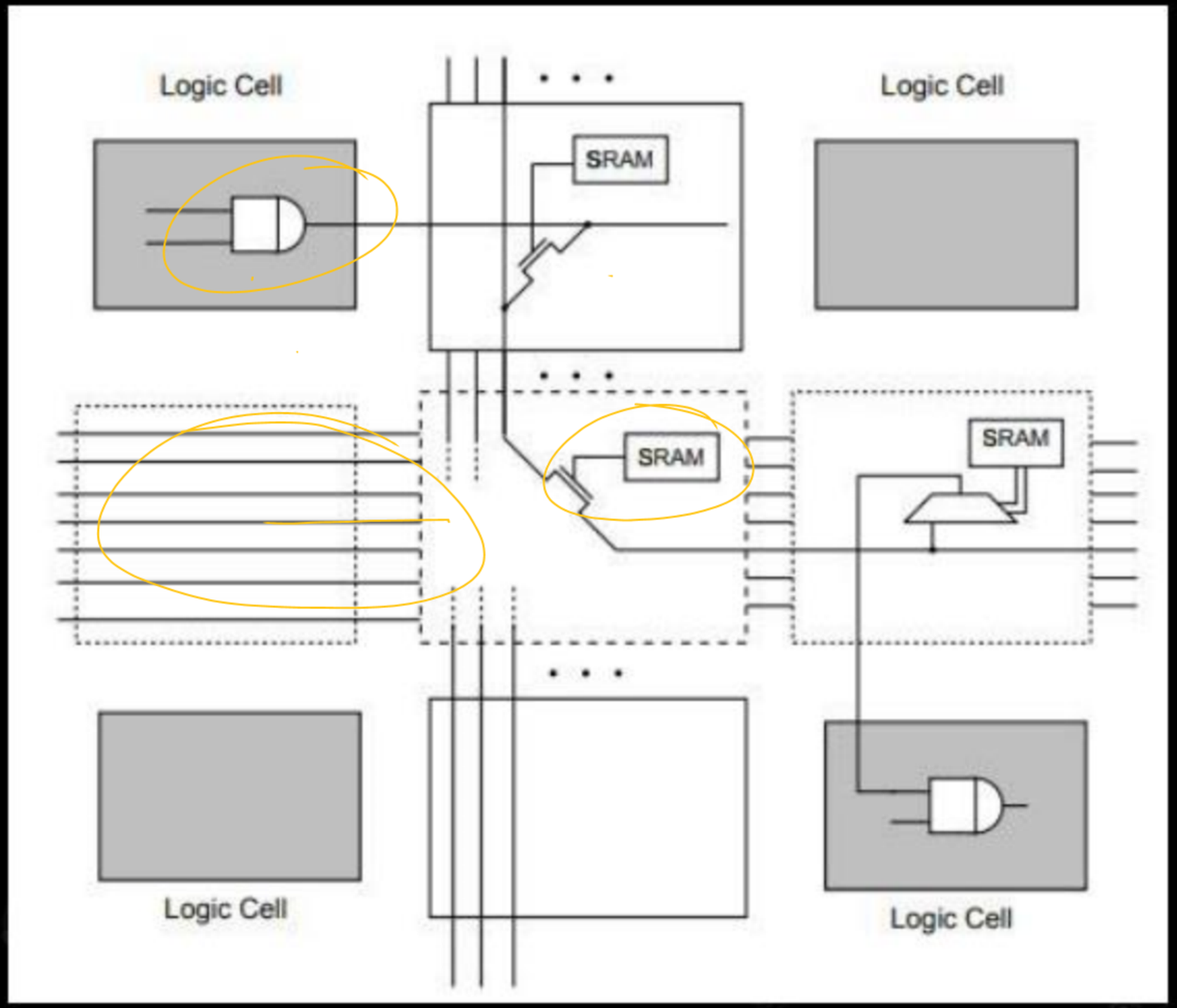
- SRAM
- EEPROM / Flash
- Anti-Fuse

SRAM

- SRAM is short form for Static RAM.
- SRAM is designed using transistors and the term static means that the value loaded on a basic SRAM Memory Cell will remain the same until deliberately changed or when the power is removed.
- A typical 6 transistor SRAM Cell to store 1 bit is shown in the following image.



- SRAM based FPGAs are used to program both the logic cells and the interconnects and they have become quite predominant due to their re-programmability and use of CMOS technology, which is known for its low dynamic power consumption, high speed and tighter integration.


Logic Cell
Logic Cell
SRAM
SRAM
SRAM
Logic Cell
Logic Cell

EEPROM / Flash

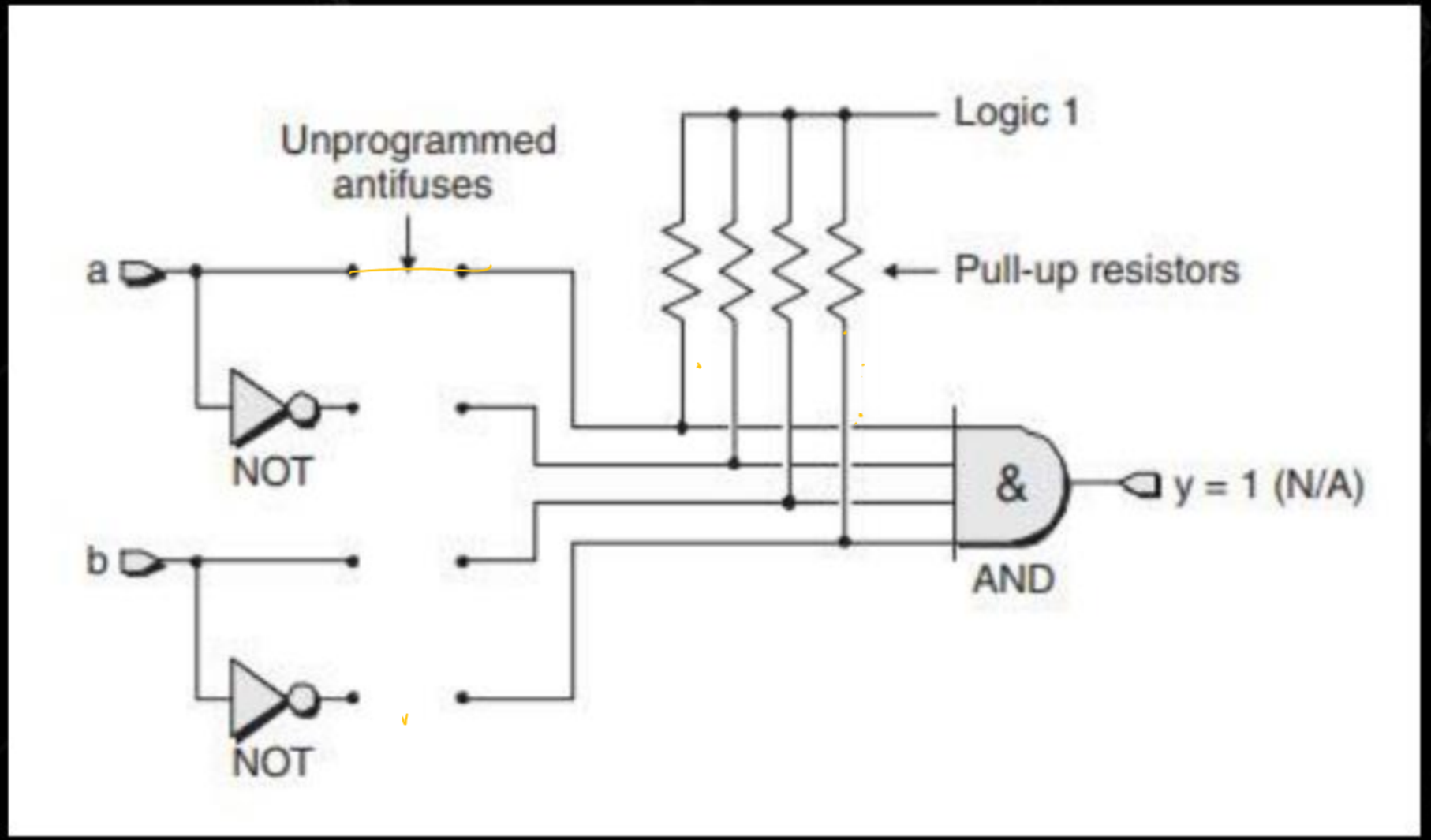
- A close alternative to SRAM based programming technology is based on EEPROM or Flash programming technologies.
- The main advantage of flash-based programming is its non-volatile nature.
- Even though flash supports re-programmability, the number of times this can be done is very small when compared to an SRAM technology.

GW
GATEWAY CLASSES

Anti-Fuse

GW
GATEWAY CLASSES

- The anti-fuse programming technology is an old technique of producing one-time programmable devices.
- They are implemented using a link called the antifuse, which in its unprogrammed state has a very high resistance and can be considered an open circuit.
- When programming, a high voltage and current is supplied to the input.
- As a result, the antifuse, which is initially in the form of amorphous silicon (basically an insulator with very high resistance) linking two metal tracks, comes to life by converting to a conducting polysilicon.
- When compared to the other two technologies, the antifuse one occupies the least amount of space but comes only as one-time programmable option.


Logic 1
Unprogrammed
antifuses
Pull-up resistors
a
NOT
&
y = 1 (N/A)
b
AND
NOT

Applications

- Used to implement small to medium complex state machines and data processing tasks on small data.
- several automotive, consumer and industrial applications.
- An easy option to prototype ASIC designs as they can be easily reconfigured to test and try several variations of the hardware before finalizing the main design.
- implemented as direct competitors to some ASICs.
- can facilitate DSP operations
- embedded control applications
- used to implement a soft-core processor of any microcontroller along with custom IO capabilities.

GATEWAY CLASSES

AKTU Full Courses (Paid)

Download Gateway Classes Application

From Google Play store

All Subjects

Link in Description

Thank You