AKTU-III SEM

GATEWAY CLASSES

Digital System Design & Digital Electronics

Unit-IV

ONE SHOT



Abhilasha ma'am

DIGITAL SYSTEM DESIGN

UNIT IV:

Logic families and semiconductor memories:

TTL NAND gate,

specifications, noise margin, propagation delay, fan-in, fan-out,

tristate TTL,

ECL,

CMOS families and their interfacing,

memory elements,

concept of programmable logic devices like FPGA,

logic implementation using programmable devices

DIGITAL ELECTRONICS

- UNIT V:
- Memory & Programmable Logic Devices:
- Digital Logic Families: DTL, DCTL, TTL, ECL & CMOS etc.,
- Fan Out, Fan in, Noise Margin;
- RAM, ROM, PLA, PAL;
- Circuits of Logic Families,
- Interfacing of Digital Logic Families,
- Circuit Implementation using ROM, PLA and PAL

INTEGRATED CIRCUITS

- Integrated circuits (ICs) are chips, pieces of semiconductor material, that contain all of the transistors, resistors, and capacitors necessary to create a digital circuit or system.
- The first ICs were fabricated using Ge BJTs in 1958.
- Jack Kirby of Texas Instruments, Nobel Prize in 2000
- Robert Noyes of Fairchild Semiconductors fabricated the first Si ICs in 1959.

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Integration Levels:

- SSI Small scale integration [12 gates/chip]
- MSI Medium scale integration [100 gates/chip]
- LSI Large scale integration [1K gates/chip]
- VLSI Very large scale integration [10K gates/chip]
- ULSI Ultra large scale integration [100K gates/chip]

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Characteristics of digital circuits

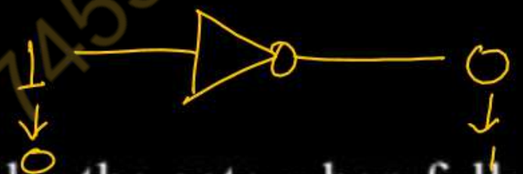
Fan in:

- Fan in is the number of inputs connected to the gate without any degradation in the voltage level.



Fan out:

- Fan out specifies the number of standard loads that the output of the gate can drive without impairment of its normal operation



Power dissipation:

- Power dissipation is a measure of power consumed by the gate when fully driven by all its inputs.

Propagation delay:

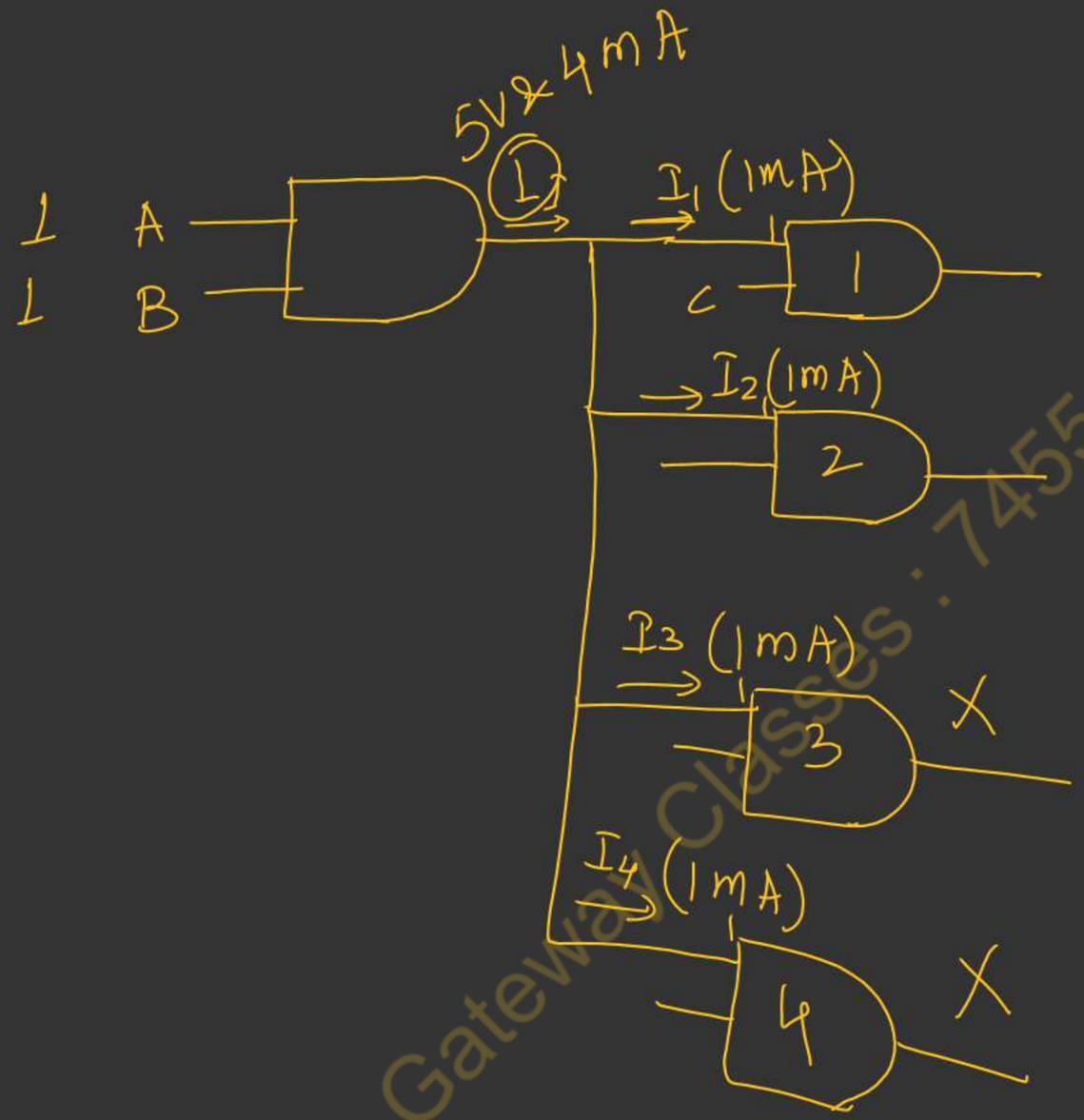
- Propagation delay is the average transition delay time for the signal to propagate from input to output when the signals change in value. It is expressed in ns.

10^{-9} sec

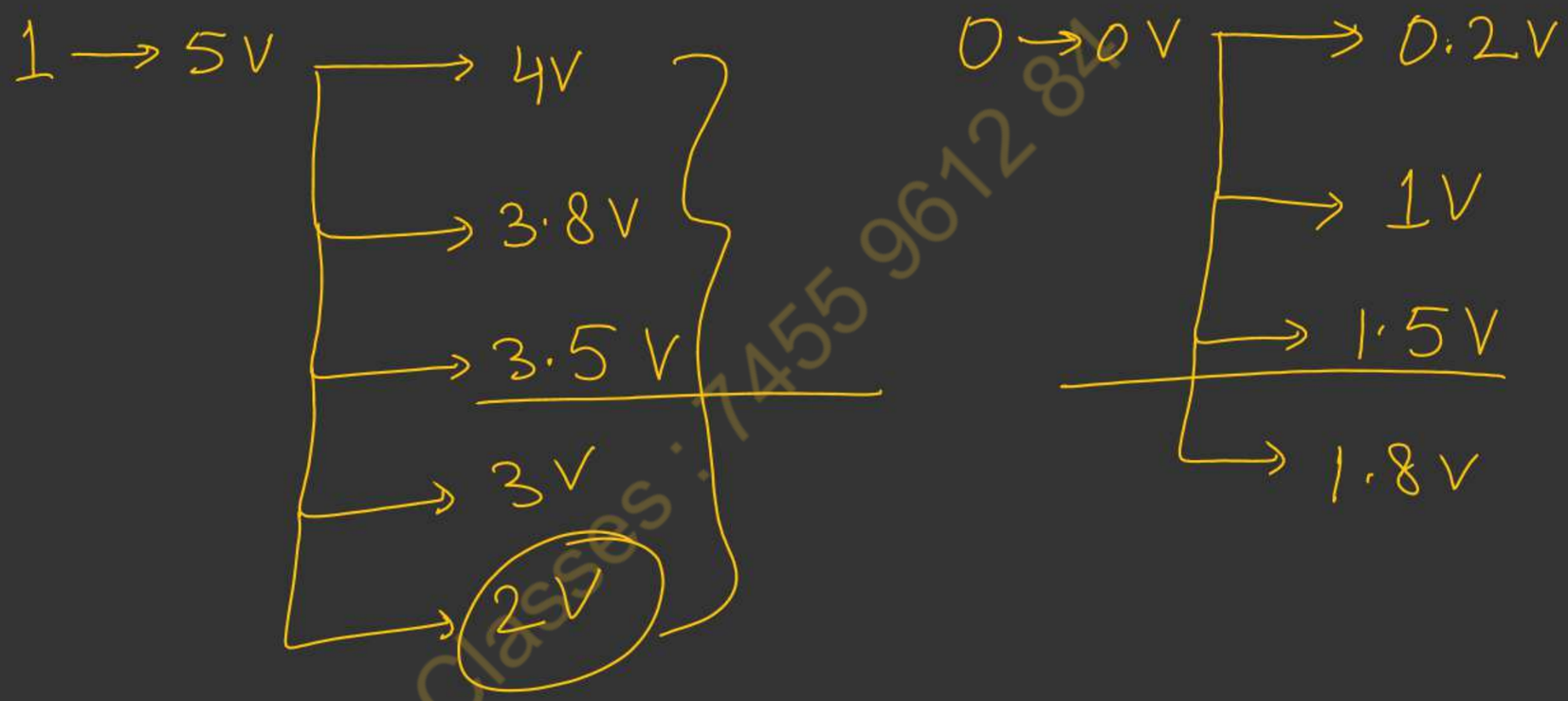
Noise margin:

- It is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output. It is expressed in volts.

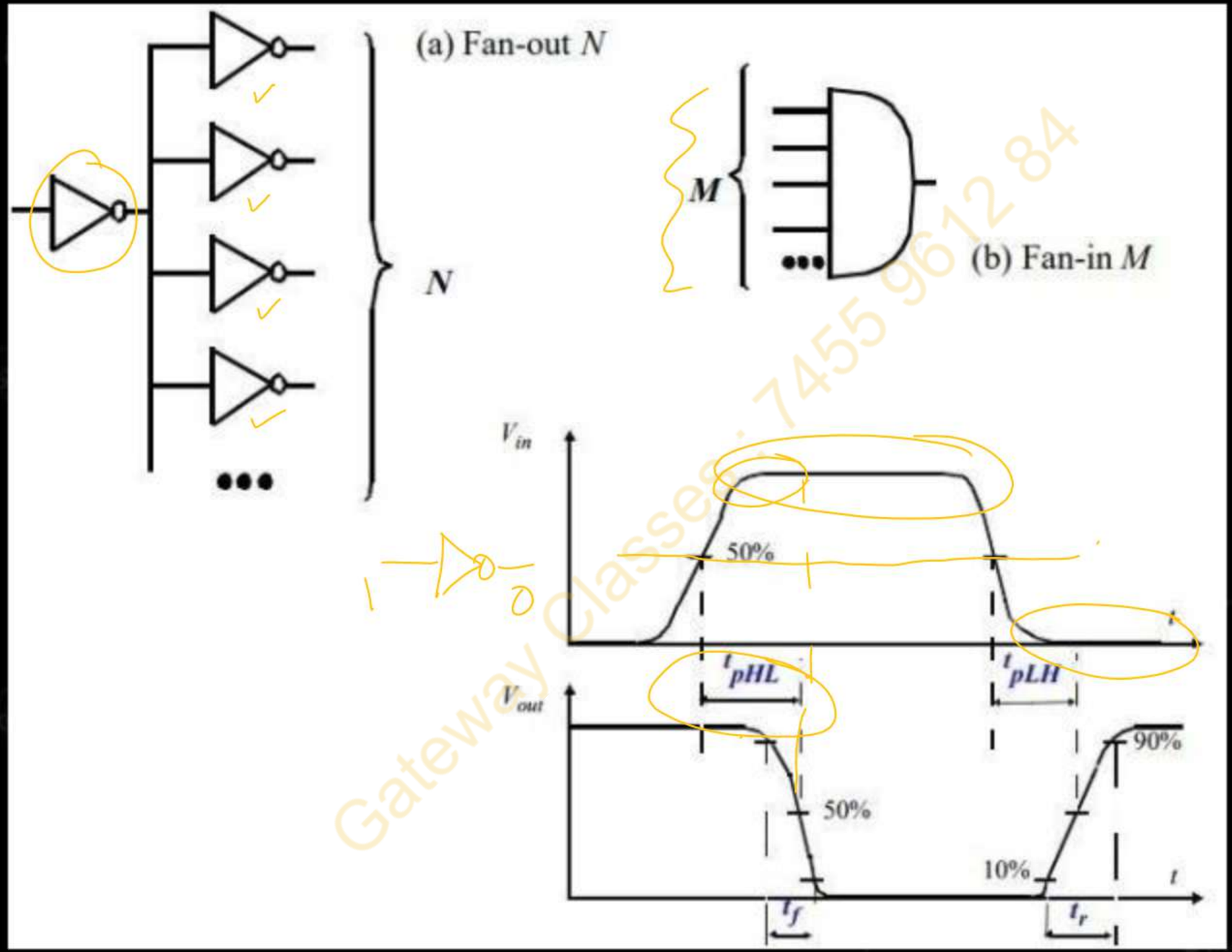
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Gateway Classes : 7455 9612 84



Gateway Classes : 7455 9612 82



Gateway Classes: 7455 9612 84

Logic Families

- Logic families are sets of chips that may implement different logical functions but use the same type of transistors and voltage levels for logical levels and for the power supplies.
- These families vary by speed, power consumption, cost, voltage & current levels.
- The most widely used families are:
- DL (Diode- logic)
- DTL （Diode-transistor logic）
- RTL （Resistor-transistor logic）
- TTL （Transistor -transistor logic）
- ECL （Emitter-coupled logic）
- MOS （Metal-oxide semiconductor）
- CMOS (Complementary Metal-oxide semiconductor）

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Digital IC Terminology

Voltage Parameters:

- V_{IH}(min): high-level input voltage, the minimum voltage level required for a logic 1 at an input.
- V_{IL}(max): low-level input voltage
- V_{OH}(min): high-level output voltage
- V_{OL}(max): low-level output voltage
- For proper operation, the input voltage levels to a logic must be kept outside the indeterminate range. Lower than VIL(max) and higher than VIH(min).



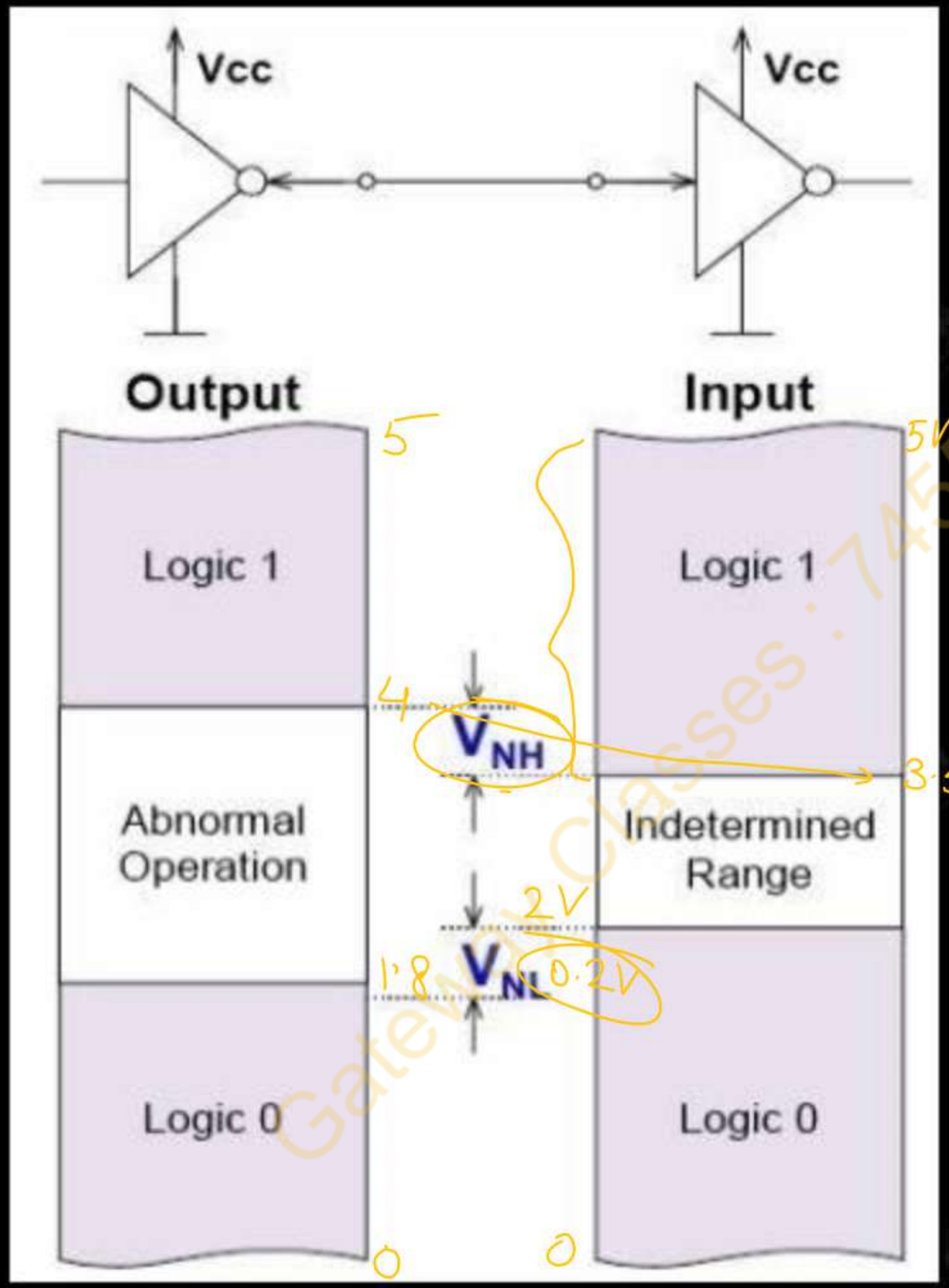
Noise Margin:

- The maximum noise voltage that can be tolerated by a circuit is termed its noise immunity (noise Margin)

Current Parameters:

- I_{OH} – Current flowing into an output in the logical "1" state under specified load conditions
- I_{OL} – Current flowing into an output in the logical "0" state under specified load conditions
- I_{IH} – Current flowing into an input when a specified HI level is applied to that input
- I_{IL} – Current flowing into an input when a specified LO level is applied to that input

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University Questions

Year	Questions	Marks
22-23 21-22 18-19	Explain FAN-IN and FAN-OUT.	2 Marks
22-23	Describe figure of merit & noise immunity of TTL & CMOS ICs	2 Marks
20-21	Define the following terms I. threshold voltage II. propagation delay III. power dissipation IV. fan-in V. fan-out	10 Marks
19-20	What is logic family? Give the classification of logic families in brief	2 Marks

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UNIVERSITY QUESTIONS

YEAR	QUESTIONS	MARKS
21-22	What do you understand by digital TTL?	2 Marks
21-22 20-21	With the help of a neat diagram, explain the working of a two-input TTL NAND gate.	10 Marks
19-20	Draw three input standard TTL NAND gate circuit and explain its operation.	10 Marks

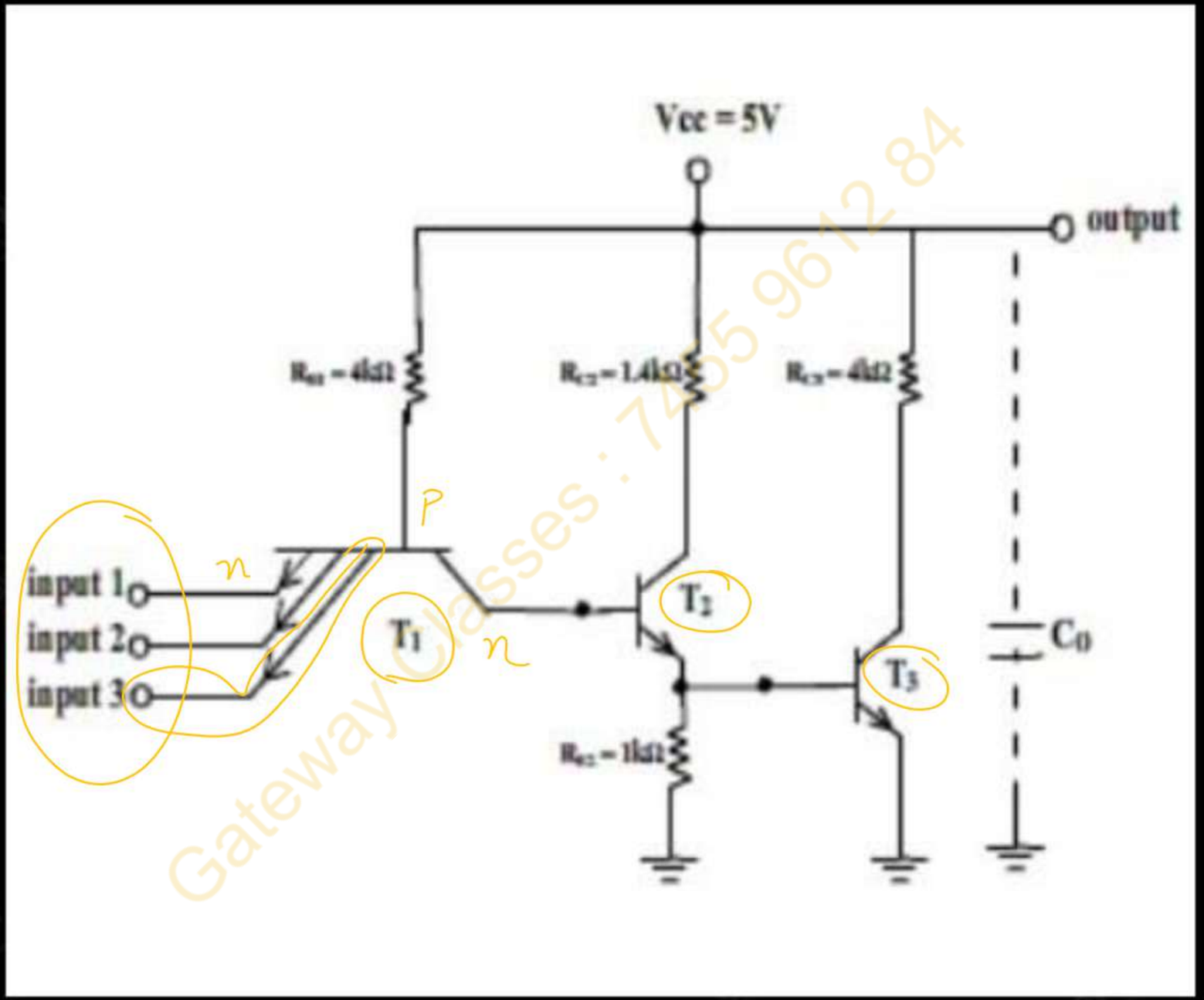
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Transistor-transistor logic (TTL)

- based on bipolar transistors one of the most widely used families of small- and medium-scale devices
- rarely used for VLSI
- typically operated from a 5V supply
- typical noise immunity about 1 – 1.6 V
- many forms, some optimised for speed, power, etc.
- High-speed versions comparable to CMOS (~ 1.5 ns)
- low-power versions down to about 1 mW/gate

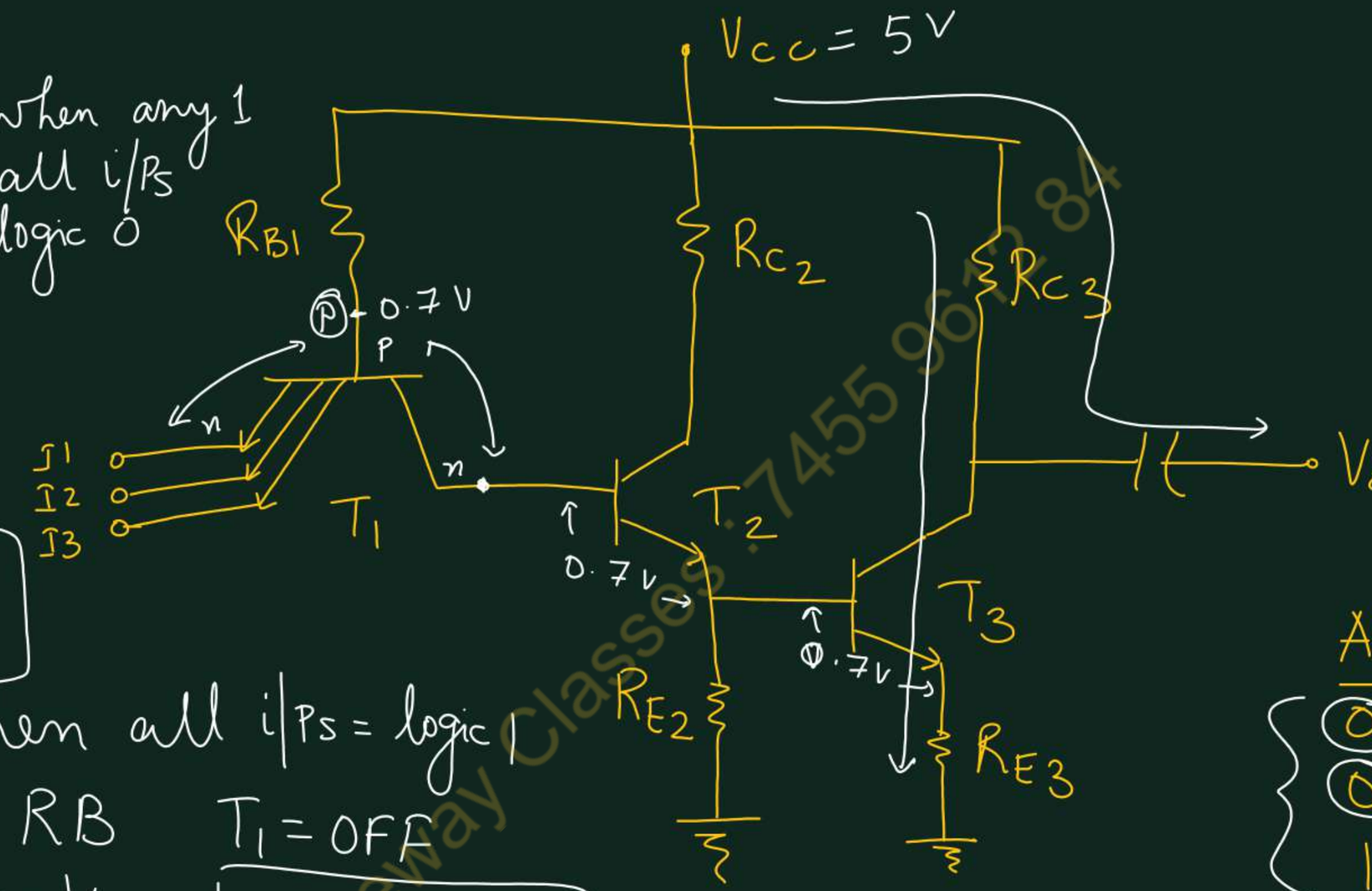
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TTL NAND Gate



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Case I : When any 1 or all i/Ps = logic 0



V_{BE_1} = FB

P = 0.7 V

So T_2 & T_3 = OFF

$V_o = V_{cc}$ = logic 1

Case II : When all i/Ps = logic 1

V_{BE1} = RB T_1 = OFF

$V_P \approx V_{cc}$

T_2 & T_3 = ON

$V_o = 0.2\,V \approx 0$ = logic 0

$Y = \overline{A \cdot B}$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

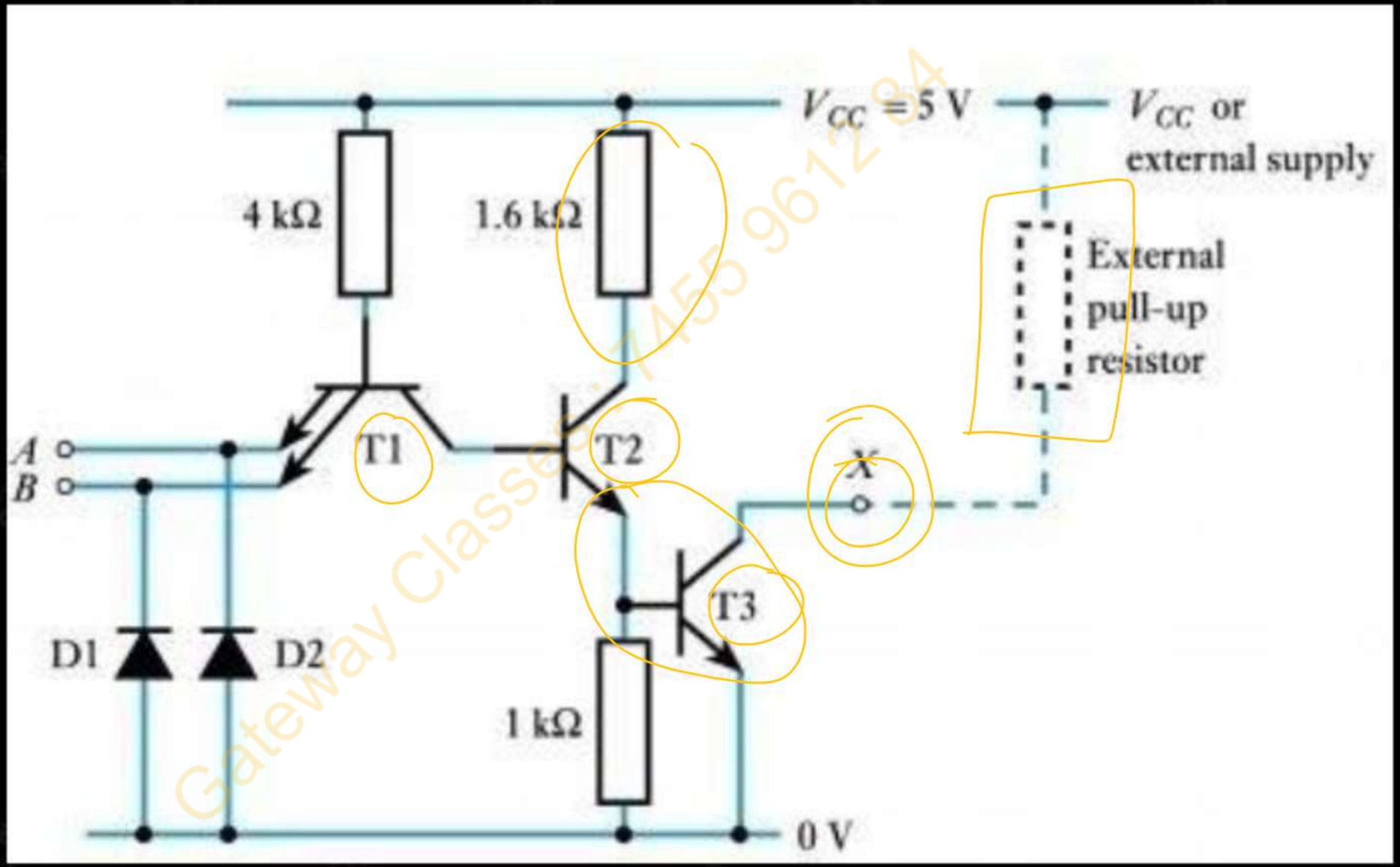
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TTL NAND Gate:

- Input terminals: The emitter of Q1 Output terminals: collector of Q2
- When any input = logic '0'
- Q1 emitter junction is forward biased. Also, its collector junction is FB,
- so Q1 goes in saturation.
- Base of Q2 is at Low voltage
- This causes base-emitter junction of Q2 to be RB, so Q2 goes in cut-off
- Hence output is 5V or logic '1'
- When all inputs = logic '1'
- Q1 emitter junction is RB. so Q1 goes in cut-off.
- Its collector voltage increases This forward biases Q2,
- so Q2 goes into saturation
- Hence output is 0V

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A TTL NAND gate with open collector output



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A TTL NAND gate with open collector output:

- Its similar to the previous circuit.
- Q2 is used as an emitter follower.
- The output of Q2 is fed to the input of Q3.
- Collector of Q2 and Q3 are in phase.
- This circuit needs an external 'Pull- up' resistor between output and power supply.
- The disadvantage of open- collector gate is their slow switching speed.
- The pull-up resistance is few kilo ohms. Gives a relatively long time constant, when multiplied by the stray output capacitance.
- Is worst when output goes from low to high.
- Open collector circuits are used to interface different families of devices that have different operating voltage levels.
- The open-collector transistor can be rated to withstand a higher voltage than the chip supply voltage.

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Applications of open-collector output:

It is used in 3 major applications:

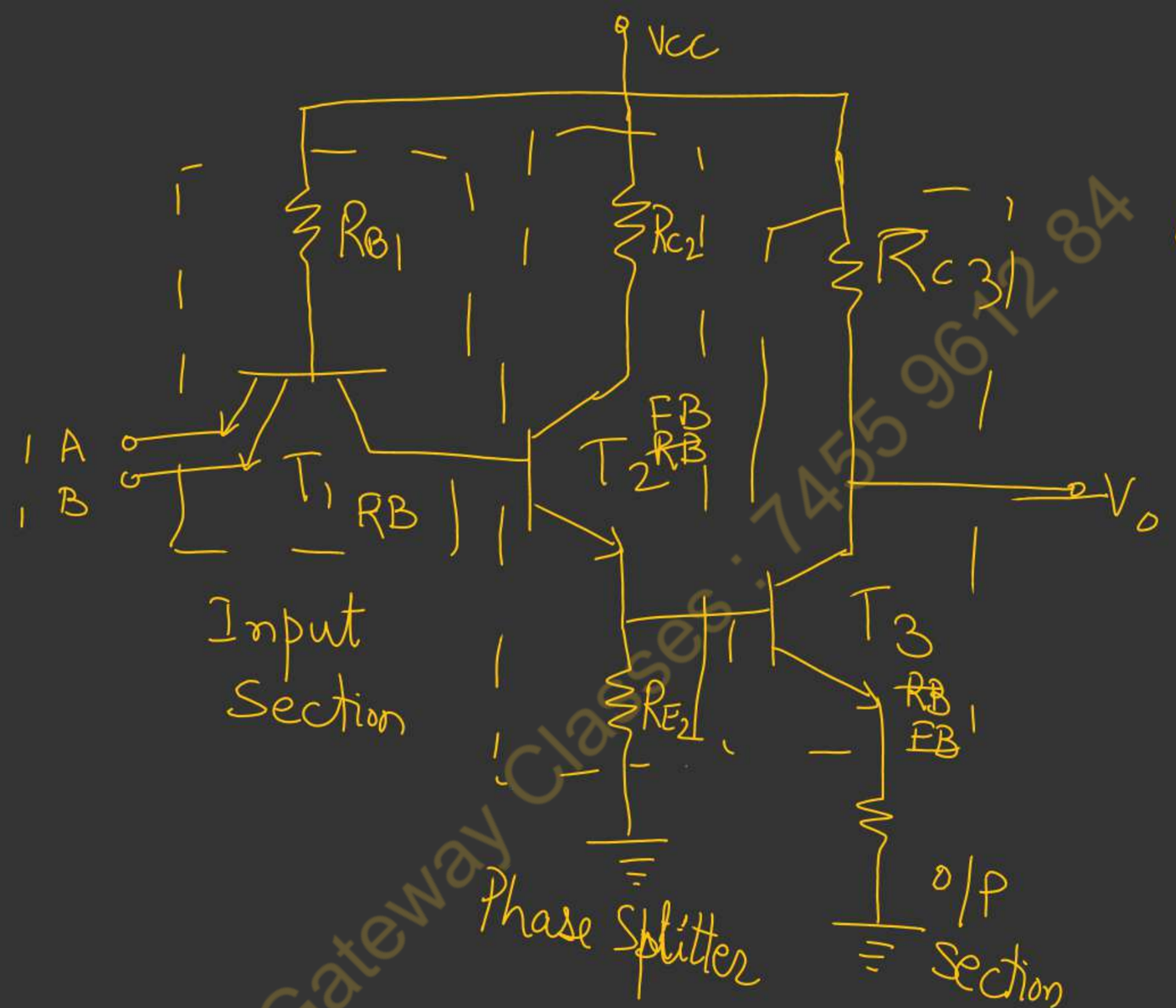
- In driving lamps or relays
- In performing wired logic
- In the construction of a common bus system

Gateway Classes : 7455 9612 84

UNIVERSITY QUESTIONS

YEAR	QUESTIONS	MARKS
21-22	What do you understand by digital TTL?	2 Marks
21-22 20-21	With the help of a neat diagram, explain the working of a two-input TTL NAND gate.	10 Marks
19-20	Draw three input standard TTL NAND gate circuit and explain its operation.	10 Marks

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Case 1 : I/P = 0

$V_o = 1$

$R_{C3} \Rightarrow$ low

Case 2 : I/P = 1

$V_o = 0$

R_{C3} = high

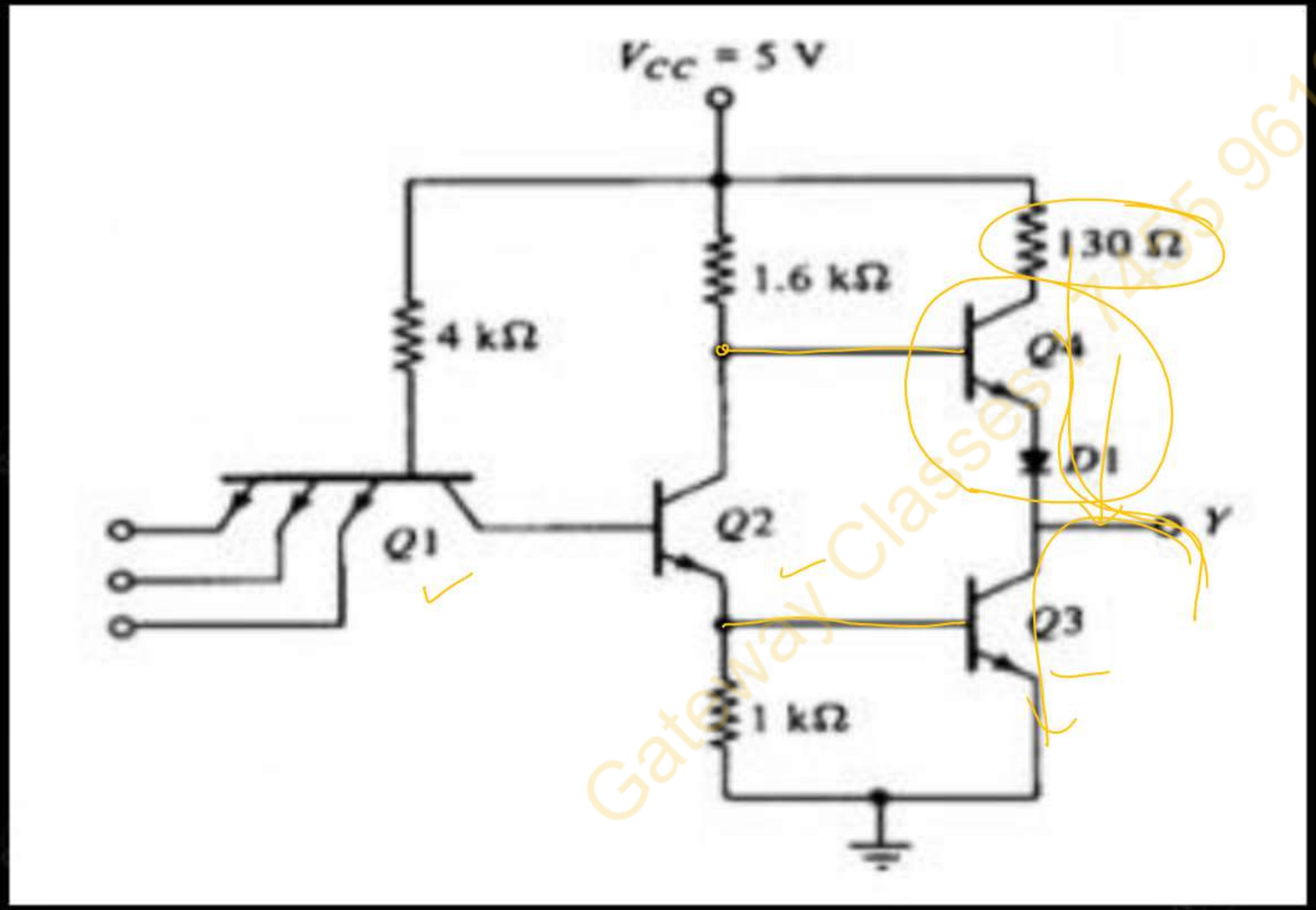
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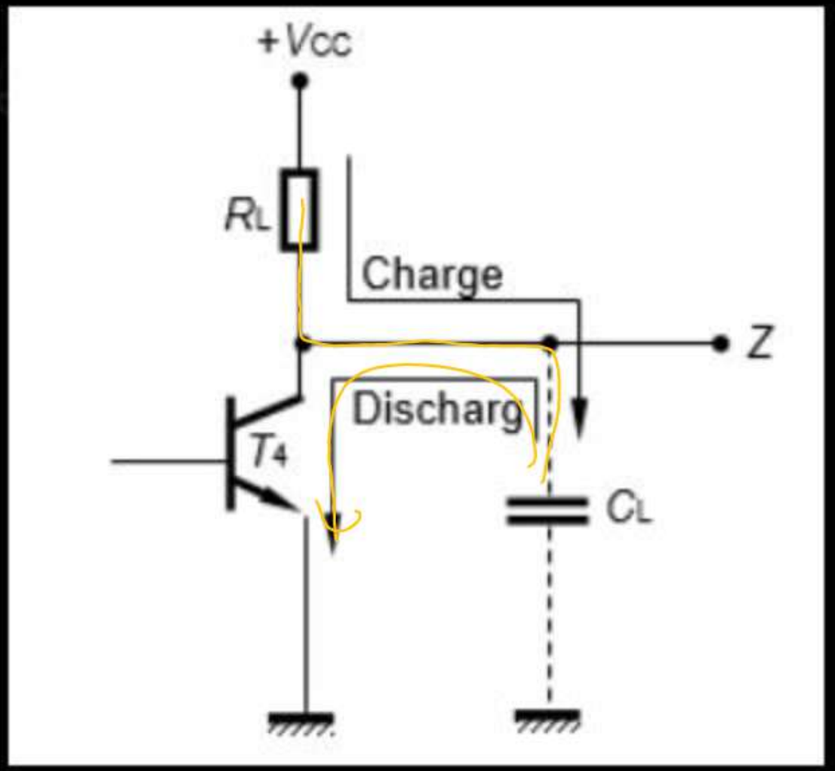
Totem pole TTL

- Totem Pole means the addition of an active pull up circuit in the output of the gate
- This results in a reduction of propagation delay.
- Logic operation is the same as the open collector output.
- The use of transistors Q4 and diode is to provide quick charging and discharging of parasitic capacitance across Q3.
- The resistor is used to keep the output current to a safe value.
- Advantages: Fast switching times due to the push-pull arrangement of the transistors. Can drive both high and low loads.
- External pull up resistor is not required.
- Disadvantage: Output of two gates cannot be tied together.

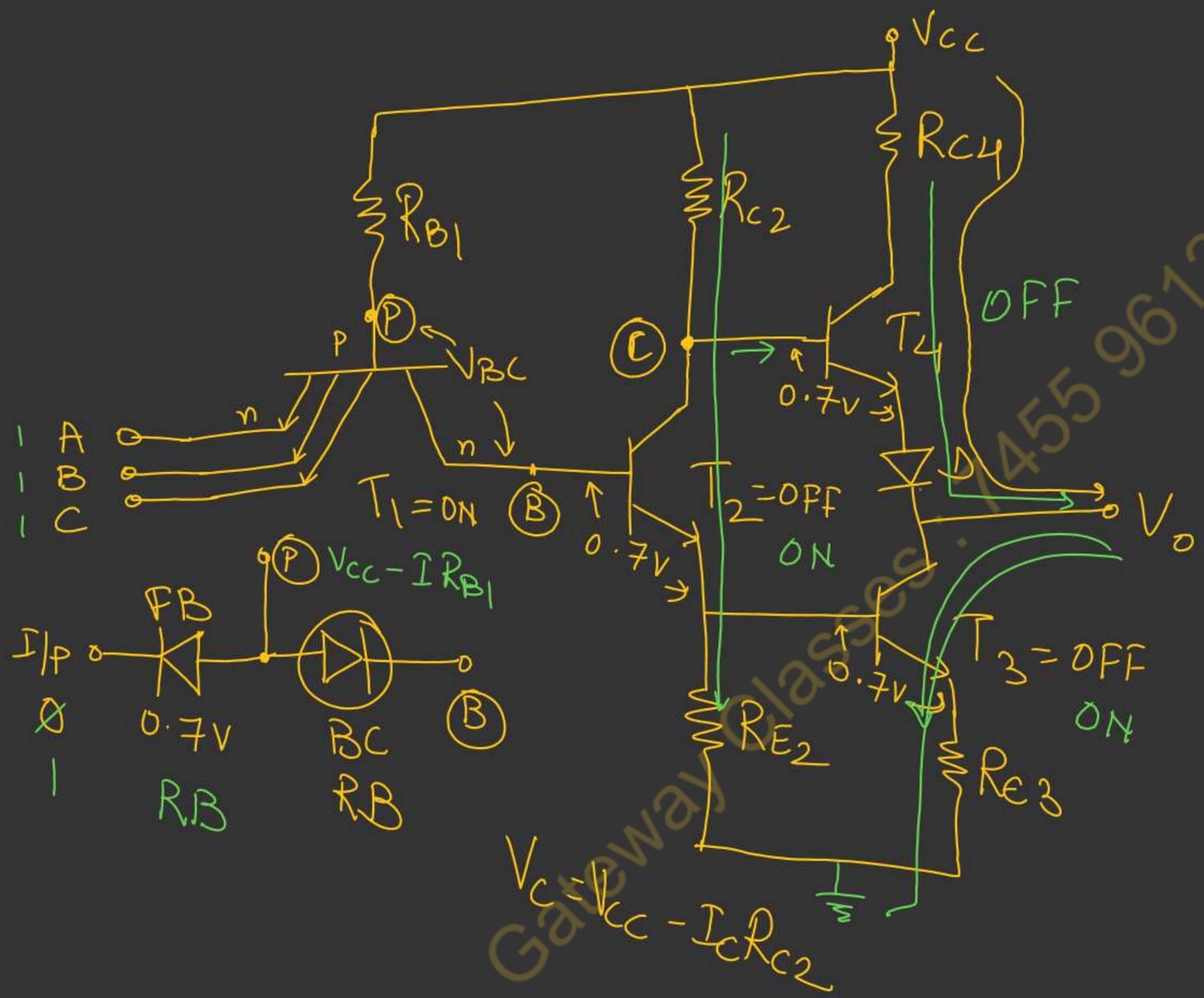
Gateway Classes : 7455 961284

Totempole TTL NAND Gate





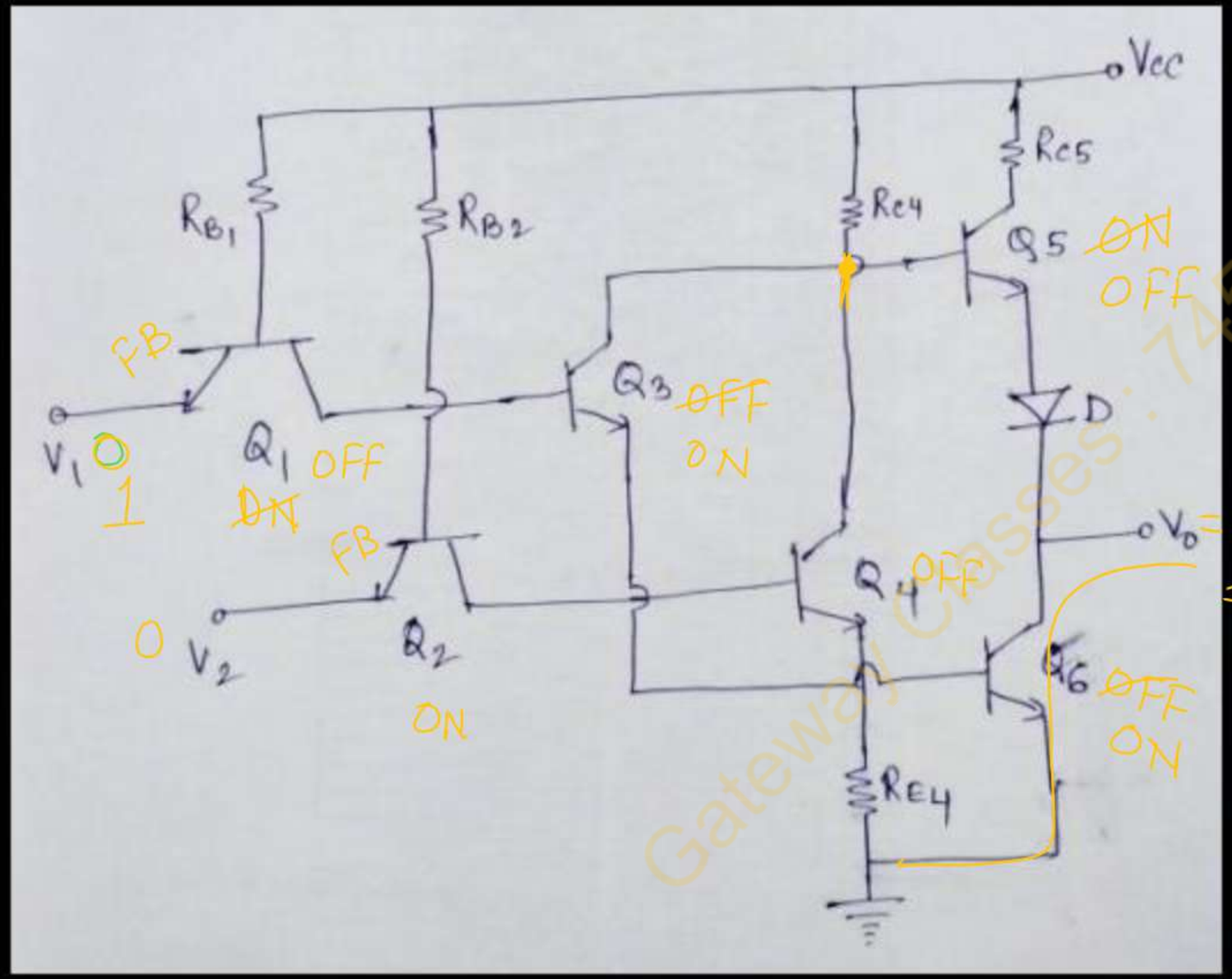
Gateway Classes 7455 9612 84



A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Gateway Classes: 1455 9612 84

Totem pole TTL NOR Gate:



NOR

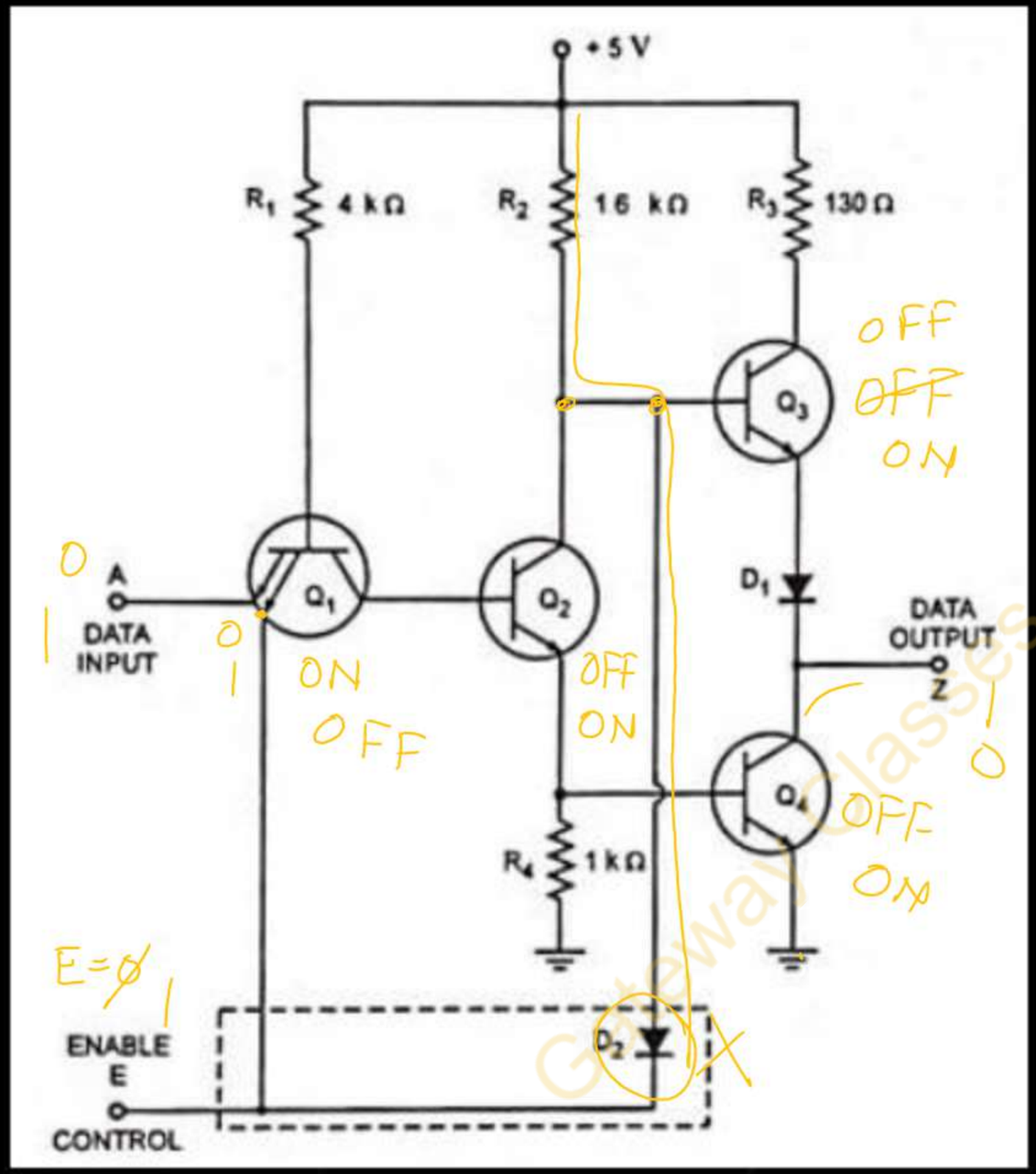
A	B	Y
0	0	1 ✓
0	1	0
1	0	0
1	1	0

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Three state Gate

- Totem-pole outputs cannot be connected together due to very large current drain from the supply and consequent heating of ICs which may get damaged.
- Open collector outputs can be connected together with a common collector resistor connected externally. This causes the problems of loading and operation speed.
- To overcome these difficulties, special circuits have been developed in which there is one more state of output, referred to as the third state or high impedance (Hi-Z) state, in addition to low and high states. Such circuits are called Tristate or three state logic.
- The tristate logic circuit utilizes the high speed operation of the totem-pole arrangement while permitting outputs to be wiredANDed (connected together).
- It provides 3 state output.
- Low-level state when a lower transistor is ON and an upper transistor is OFF.
- High-level state when the lower transistor is OFF and the upper transistor is ON.
- Third state when both transistors are OFF. It allows a direct wire connection of many outputs.

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- When E = 0, the circuit goes into its Hi-Z state regardless of the state of logic input A.
- The low at E forward-biases the emitter-base junction of transistor Q1 and shunts the resistor R1 current away from transistor Q2 so that Q2 turns off, which turns transistor Q4 off.
- The low at E also forward biases diode D2 to shunt current away from the base of transistor Q3, so that Q3 also turns off.
- With both totem-pole transistors in the off-state, the output terminal is essentially an open circuit.

Gateway Classes : 7455 961 284

Truth Table for TTL Inverter

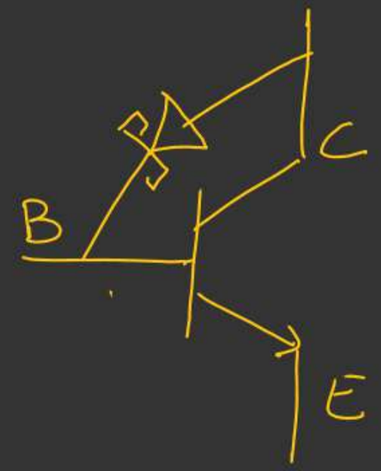
Data Input (A)	Control (E)	Data Output
0	0	High Z
1	0	High Z
0	1	1
1	1	0

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Schottky TTL

- A relatively fast bipolar logic family
- Its internal configuration is similar to normal TTL except that Schottky transistors are used.
- Schottky transistors consist of a normal bipolar transistor with a Schottky diode connected across the base-collector junction.
- The Schottky diode is a semiconductor-metal diode that has a low cut-in voltage (forward bias voltage drop), typically 300 millivolts.
- It has a relatively high switching speed.
- In Schottky TTL the low cut-in voltage of the diode limits the base-collector voltage to about 400 mV, which prevents the transistor falling into saturation.
- This results in faster switching times for the transistors constructed in this way.

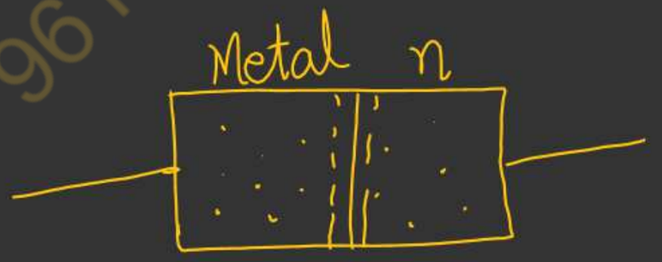
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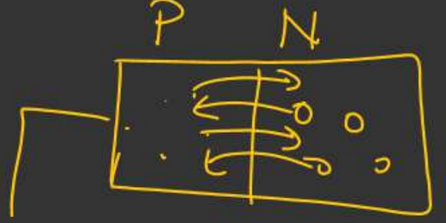


Simple Xtor + Shottky diode

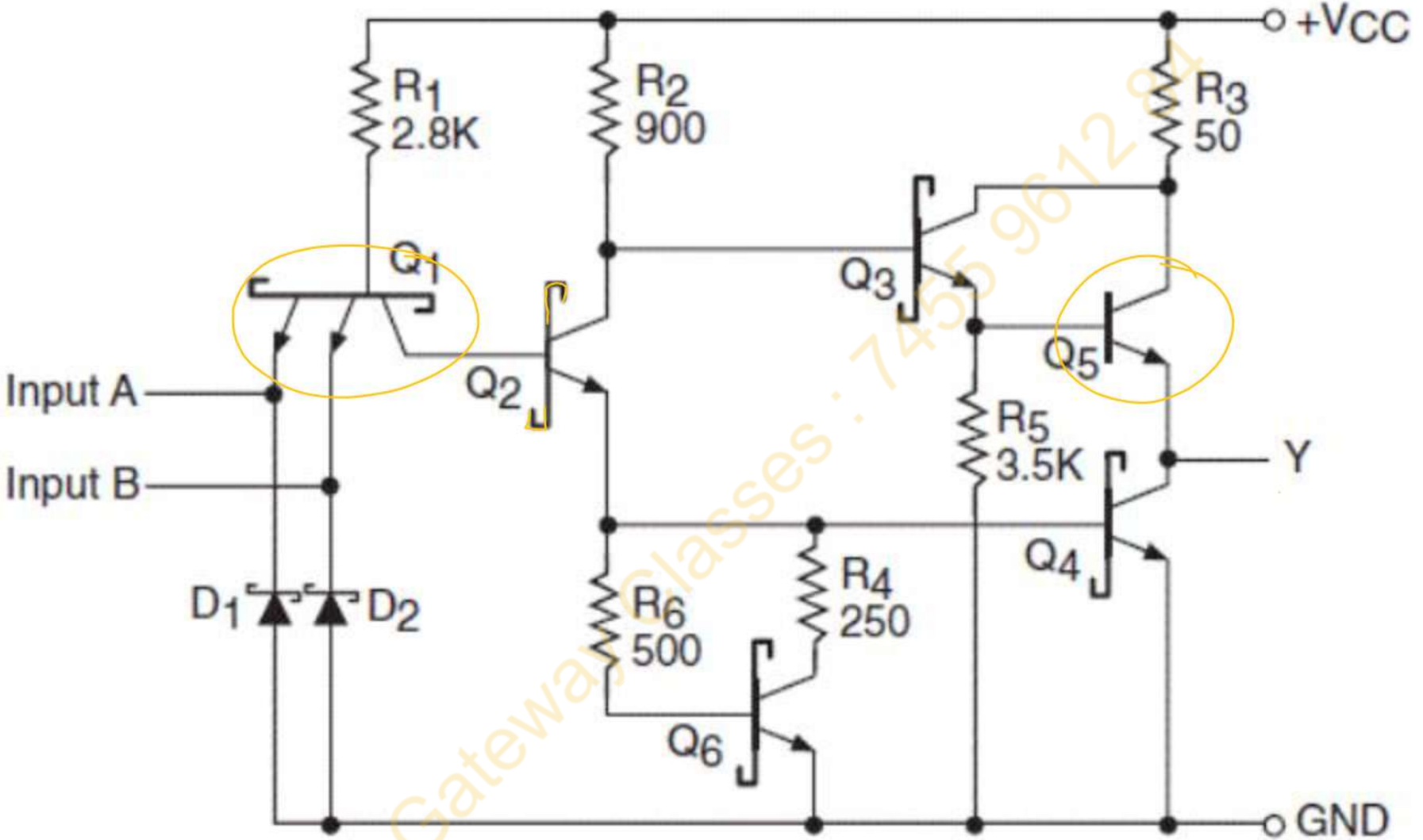


Shottky Transistor





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+Vcc
R1
2.8K
R2
900
R3
50
Q1
Q2
Q3
Q5
Input A
Input B
R5
3.5K
Y
D1
D2
R6
500
R4
250
Q4
Q6
GND

UNIVERSITY QUESTIONS

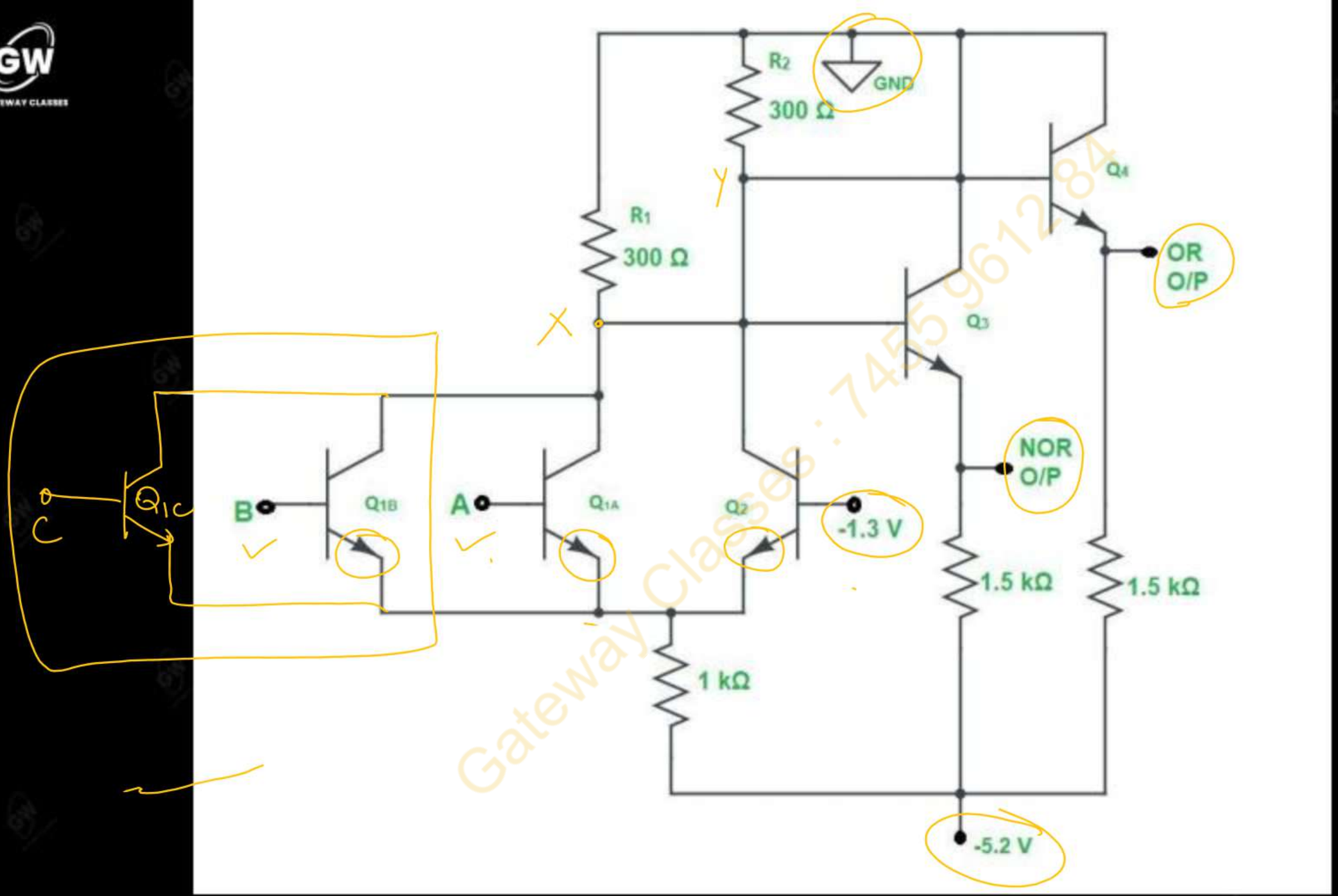
YEAR	QUESTIONS	MARKS
22-23	Draw and Explain a NAND gate in Totem Pole TTL Configuration.	10 Marks

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Emitter-coupled logic

- high-speed integrated circuit
- bipolar transistor logic family
- uses an overdriven BJT differential amplifier with single-ended input
- limited emitter current to avoid the saturated (fully on) region of operation
- slow turn-off behavior
- As the current is steered between two legs of an emitter-coupled pair, ECL is sometimes called current-steering logic (CSL), current-mode logic (CML) or current-switch emitter-follower (CSEF) logic.
- Disadvantage: each gate continuously draws current, which means that it requires (and dissipates) significantly more power than those of other logic families, especially when quiescent.

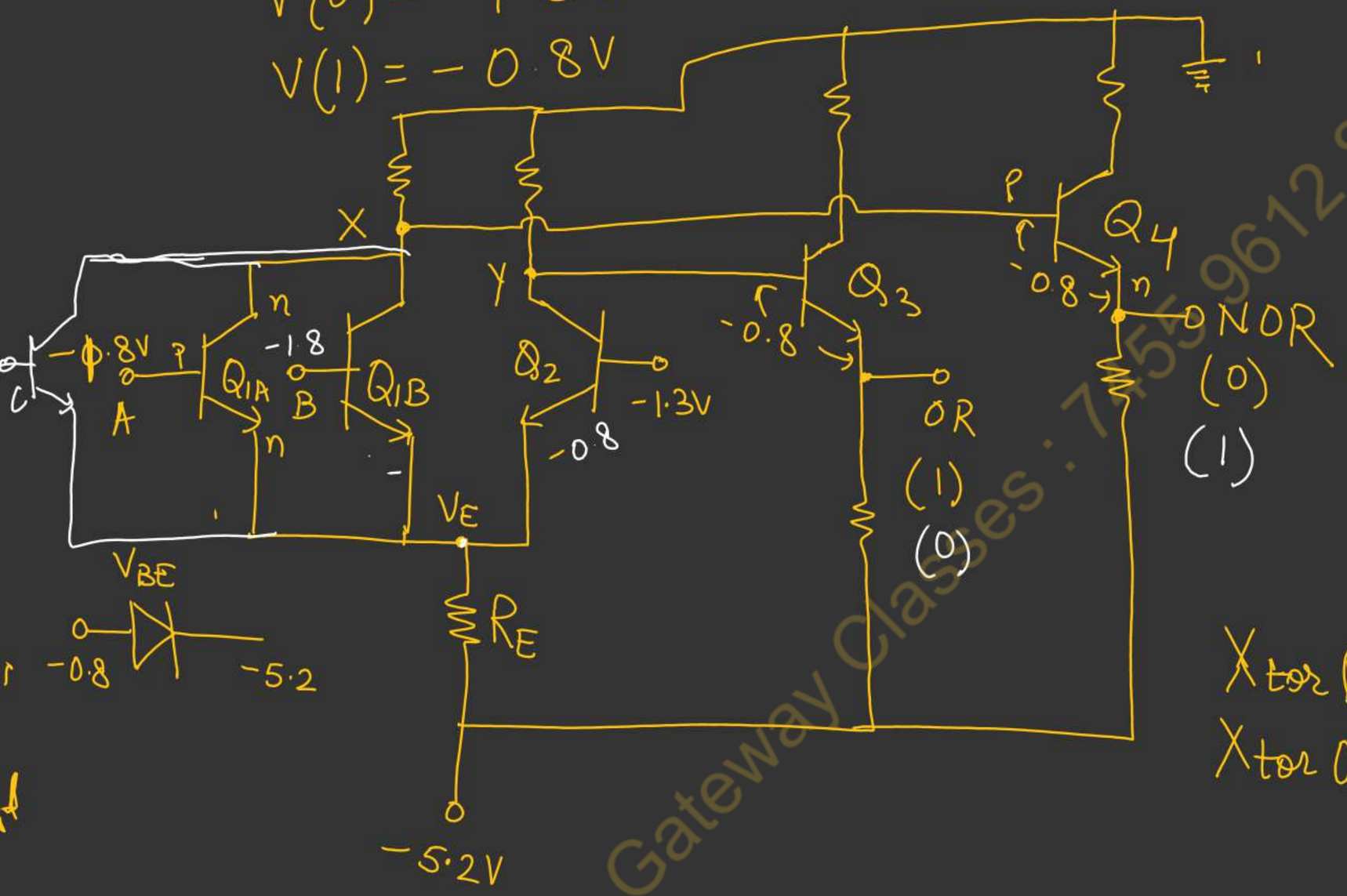
Gateway Classes : 7455 9612 84



Gateway Classes : 7455 961284

$V(0) = -1.8V$

$V(1) = -0.8V$



A	B	NOR	OR
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

X_{tor} OFF $\rightarrow V_C = 0V$

X_{tor} ON $\rightarrow V_C = -1V$

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Case 1: When any 1 or all i/Ps are at logic 1

Respective $V_{BEQ_1} = FB = -0.8V$

$V_E = -0.8 - 0.8 = -1.6V$

$V_{BE_{Q_2}} = -1.6 - (-1.3) = -0.3V$

So Q_2 = OFF (RB)

$Y = 0V$ $\quad X = -1V$

$V_{EQ_3} = 0 - 0.8V = -0.8V = \text{logic } 1$

$V_{EQ_4} = -1 - 0.8 = -1.8V = \text{logic } 0$

Case 2: When all i/Ps are at logic 0

Q_{1A} & Q_{1B} = OFF $\quad Q_2$ = ON

$V_E = -1.3V - 0.8V = -2.1V$

$V_{BEQ_1} = -2.1 - (-1.8) = -0.3V$

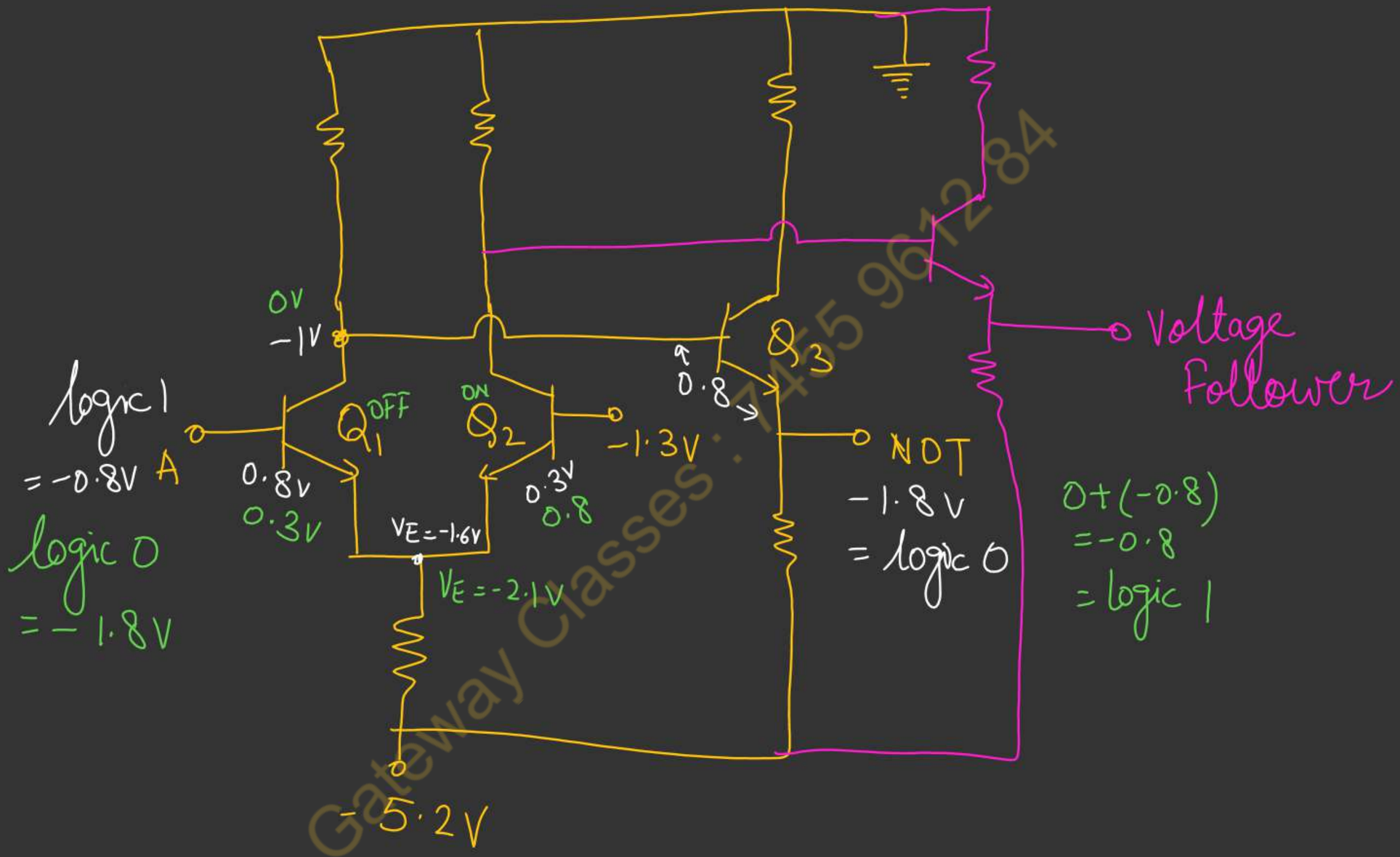
So Q_{1A} & Q_{1B} = OFF

$X = 0$ $\quad Y = -1V$

$V_{EQ_4} = X + (-0.8) = 0 + (-0.8) = -0.8 = \text{logic } 1$

$V_{EQ_3} = Y + (-08) = -1 + (-0.8) = -1.8 = \text{logic } 0$

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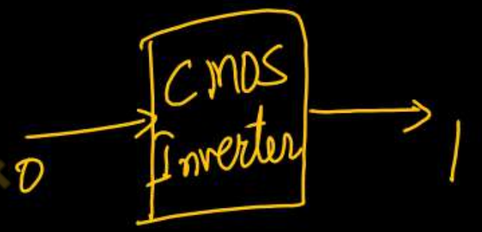
Gateway Classes : 7455 961284

UNIVERSITY QUESTIONS

YEAR	QUESTIONS	MARKS
22-23 19-20	Describe figure of merit & noise immunity of TTL & CMOS ICs	2 Marks
22-23	Draw CMOS inverter circuit and explain its working.	10 Marks
21-22	Draw a circuit diagram of a CMOS inverter. Draw its transfer characteristics and explain its operation.	10 Marks
20-21	With the help of a neat diagram, explain the working of any two I. a CMOS inverter, II. a two input CMOS NAND gate III. a two input CMOS NOR gate	10 Marks
19-20	Compare TTL and CMOS logic families and also draw CMOS NOR gate.	10 Marks

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CMOS Technology



- Stands for "Complementary Metal Oxide Semiconductor."
- It is a technology used to produce integrated circuits.
- CMOS circuits are found in several types of electronic components, including microprocessors, batteries, and digital camera image sensors.
- Fabrication process that uses complementary and symmetrical pairs of p-type and n-type MOSFETs for logic functions.
- Two important characteristics of CMOS devices are high noise immunity and low static power consumption.
- Since one transistor of the MOSFET pair is always off, the series combination draws significant power only momentarily during switching between on and off states.
- CMOS devices do not produce as much waste heat as other forms of logic.
- These characteristics allow CMOS to integrate a high density of logic functions on a chip.
- The most widely used technology to be implemented in VLSI chips.

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Difference between CMOS and TTL

Characteristics	CMOS	TTL
Voltage Levels	Wide range of voltage levels	Fixed voltage levels (typically 5V)
Power Consumption	Low	High
Technology	MOSFET	Bipolar Junction Transistor (BJT)
Noise Immunity	High	Low
Fan-Out Capability	High fan-out capability	Lower fan-out capability
Speed	Slow propagation delays	Fast propagation delays
Power Supply	Typically operates at 5V or 3.3V	Typically operates at 5V
Applications	Battery-operated devices, high-density ICs	High-speed applications, memory systems

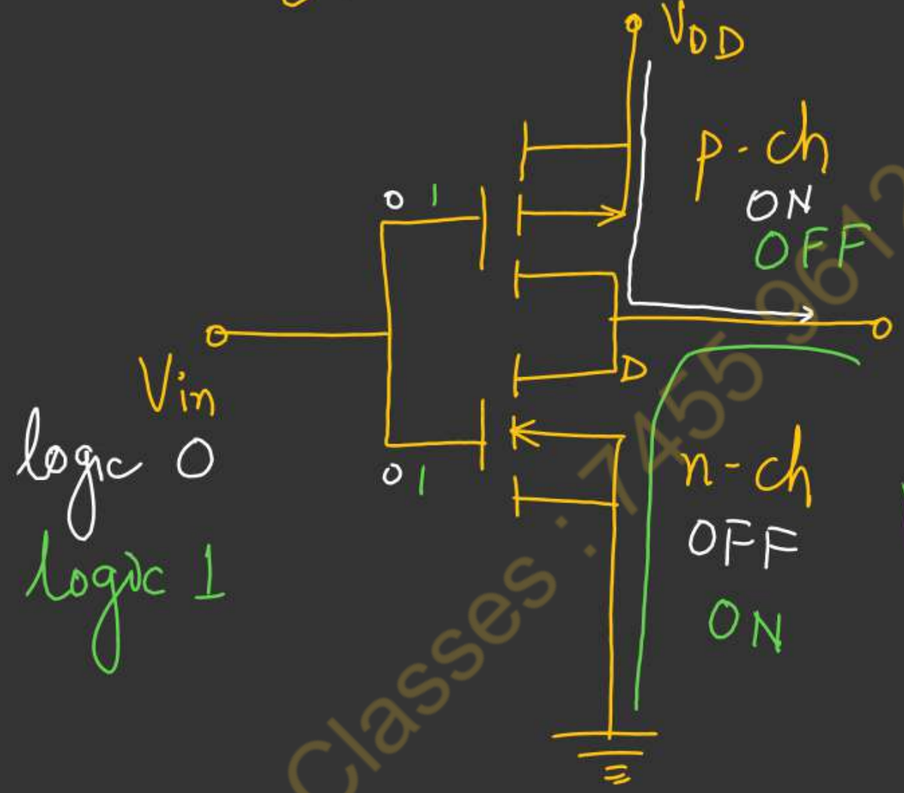
Gateway Classes : 7455 961 084

CMOS Inverter

- CMOS inverter are some of the most widely used and adaptable MOSFET inverters used in chip design.
- They operate with very little power loss and at relatively high speed.
- CMOS inverter has good logic buffer characteristics & its noise margins in both low and high states are large.
- A CMOS inverter contains a PMOS and a NMOS transistor connected at the drain and gate terminals, a supply voltage VDD at the PMOS source terminal, and a ground connected at the NMOS source terminal.
- V_{IN} is connected to the gate terminals and V_{OUT} is connected to the drain terminals.
- As the voltage at the input of the CMOS device varies between 0 and 5 volts, the state of the NMOS and PMOS varies accordingly.
- When V_{IN} is low, the NMOS is "off", while the PMOS stays "on": instantly charging V_{OUT} to logic high.
- When Vin is high, the NMOS is "on and the PMOS is "off" draining the voltage at V_{OUT} to logic low.

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CMOS Inverter



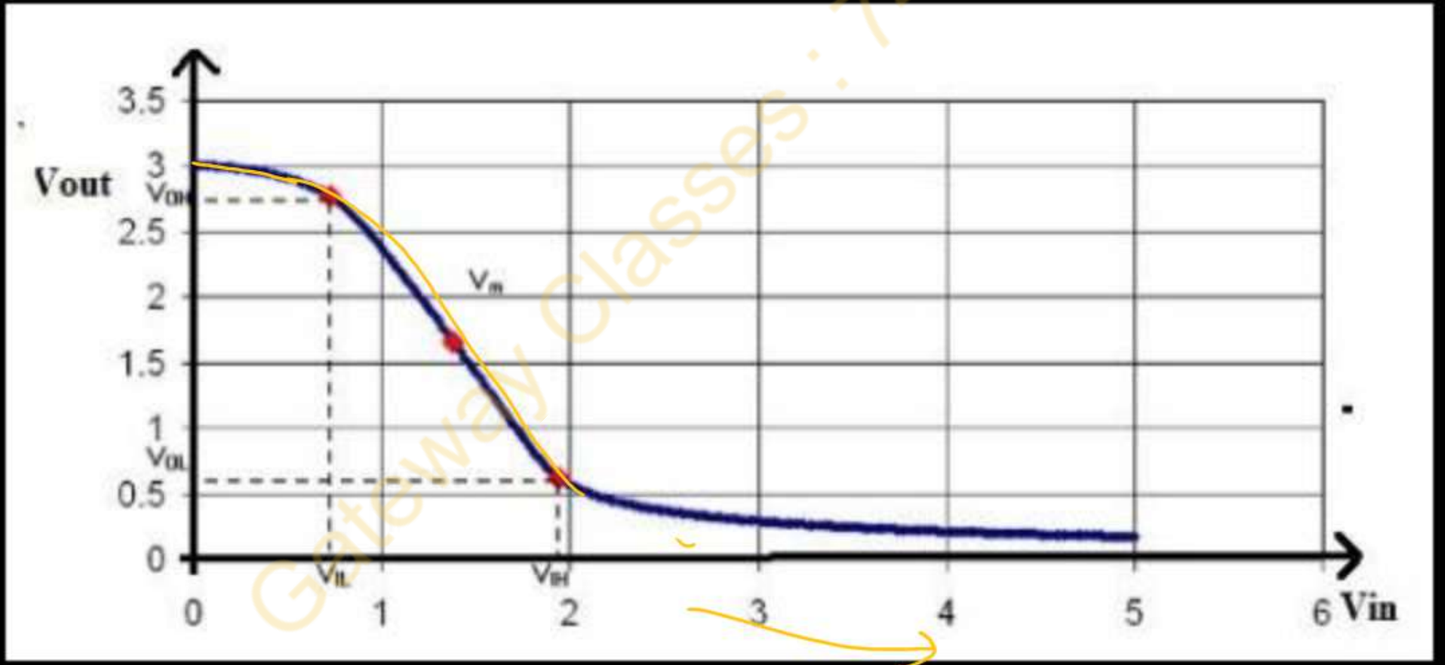
p-ch i/p = 0
⇒ ON

n-ch i/p = 1
⇒ ON

Gateway Classes : 7455 9612 84

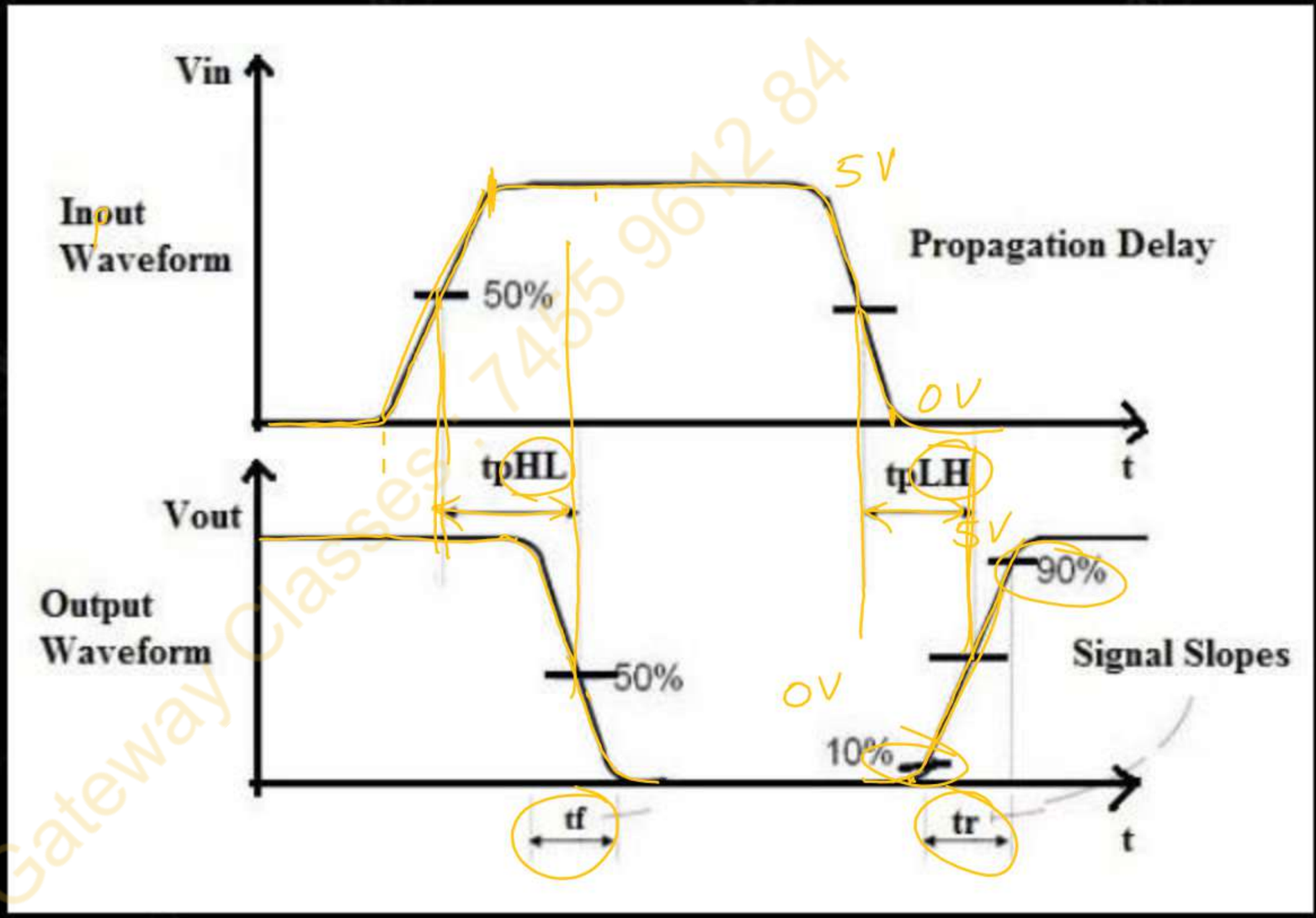
Inverter Static Characteristics or VTC

- The quality of the inverter can be measured frequently by using the VTC or voltage transfer curve, which is plotted between input voltage (Vin) and output voltage (Vo).
- From the following static characteristics, the parameters of devices like gain, operating logic levels & noise tolerance, and noise can be obtained.
- The transition region slope is a measure of quality – steep slopes yield exact switching.



Gateway Classes : 7455 961 264

Inverter Dynamic Characteristics



Gateway Classes: 7455 9612 84

Inverter Dynamic Characteristics

- Rise Time or tr: Rise time is the time used to increase the signal from 10% to 90%.
- Fall Time or tf: Fall time is the time used to drop the signal from 90% to 10%
- Edge Rate or trf : It is (tr + tf)/2.
- The propagation delay from high to low or tpHL: The time used to drop from VOH – 50%.
- The propagation delay from low to high or tpLH: The time used to increase from 50%- VOL.
- Propagation Delay or tp: It is (tpHL + tpLH)/2.
- Contamination Delay or tcd: It is the smallest time from the 50% input crossing to the 50% output crossing.

Gateway Classes :7455961284

Advantages

- The CMOS inverter's steady-state power dissipation is negligible virtually, apart from small power dissipation because of leakage currents.
- The VTC (voltage transfer characteristic) exhibits a complete o/p voltage swing in between 0 V & VDD, and the transition of voltage transfer characteristic is normally very sharp. Thus, the characteristics of the CMOS inverter look like an ideal inverter.
- These inverters use electricity once they are switched ON & OFF resulting in less power consumption. As a result, these inverters generate extremely less waste heat to make them highly efficient, so used in small and delicate electronic devices.
- These inverters include high noise immunity, which lets them block both incoming & outgoing frequency spikes.
- These are low-cost to produce mass.

Gateway Classes: 7459061284

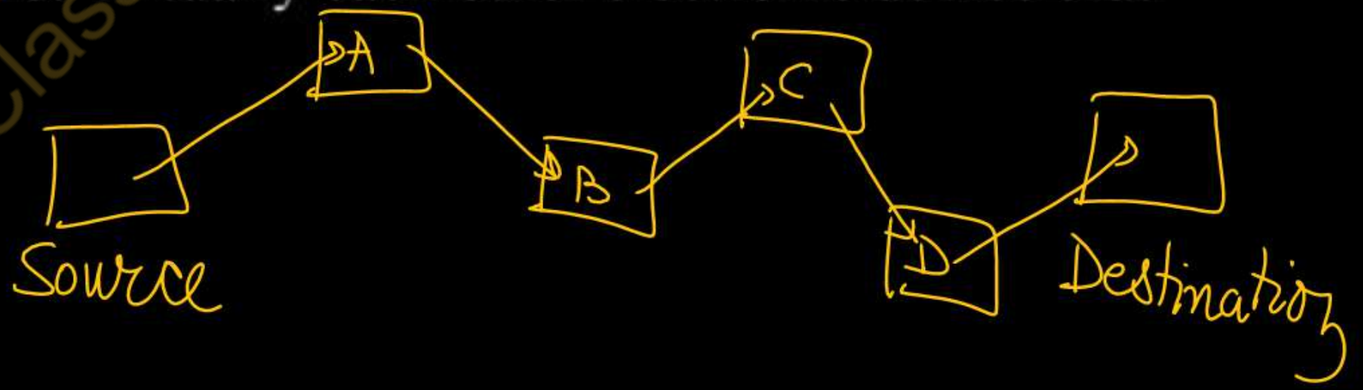
Disadvantages

- As compared to other inverters, the switching speed of the CMOS inverter is high.
- These are very difficult to fabricate due to both the transistors used on the same Silica piece.
- It uses two transistors to make an inverter, so it uses more space on the IC as compared to the NMOS inverter.

Gateway Classes : 7455 96 10 84

Applications

- CMOS inverters are used in different ICs (integrated circuits) like microprocessors, static RAM, microcontrollers, data converters, image sensors & transceivers.
- These are found in mobile devices, digital cameras, home computers, cell phones, routers, network servers, modems & virtually each other electronic device that needs logic functions.



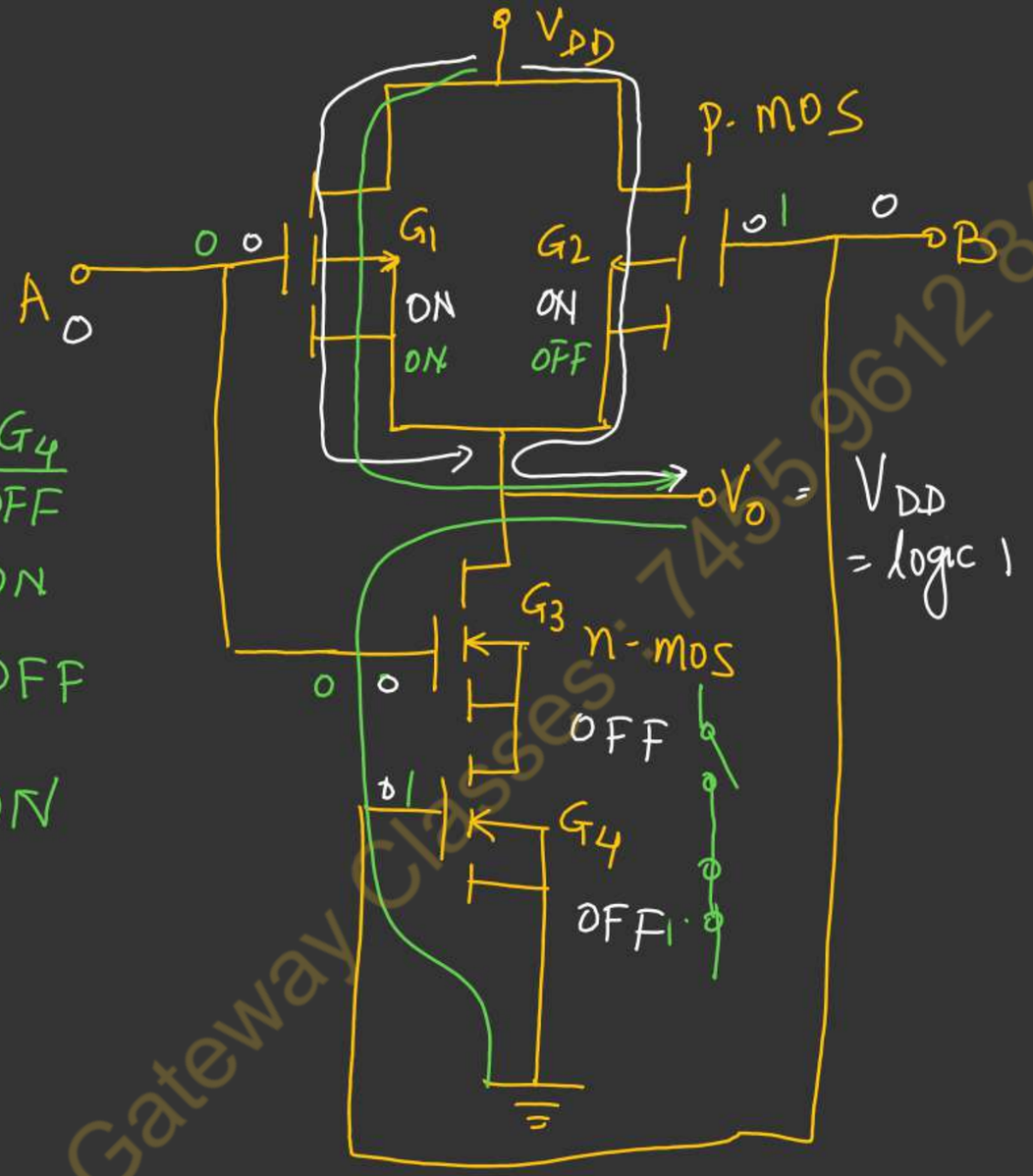
Gateway Classes: 7455 961284

CMOS NAND Gate

- It consists of two series NMOS transistors between Y and Ground and two parallel PMOS transistors between Y and V_{DD} .
- If either input A or B is logic 0, at least one of the NMOS transistors will be OFF, breaking the path from Y to Ground. But at least one of the PMOS transistors will be ON, creating a path from Y to V_{DD} . Hence, the output Y will be high.
- If both inputs are high, both of the NMOS transistors will be ON and both of the PMOS transistors will be OFF. Hence, the output will be logic low.

A	B	Pull Down network	Pull Up network	Output Y
0	0	OFF	ON	1
0	1	OFF	ON	1
1	0	OFF	ON	1
1	1	ON	OFF	0

Gateway Classes: 7455 0912 84



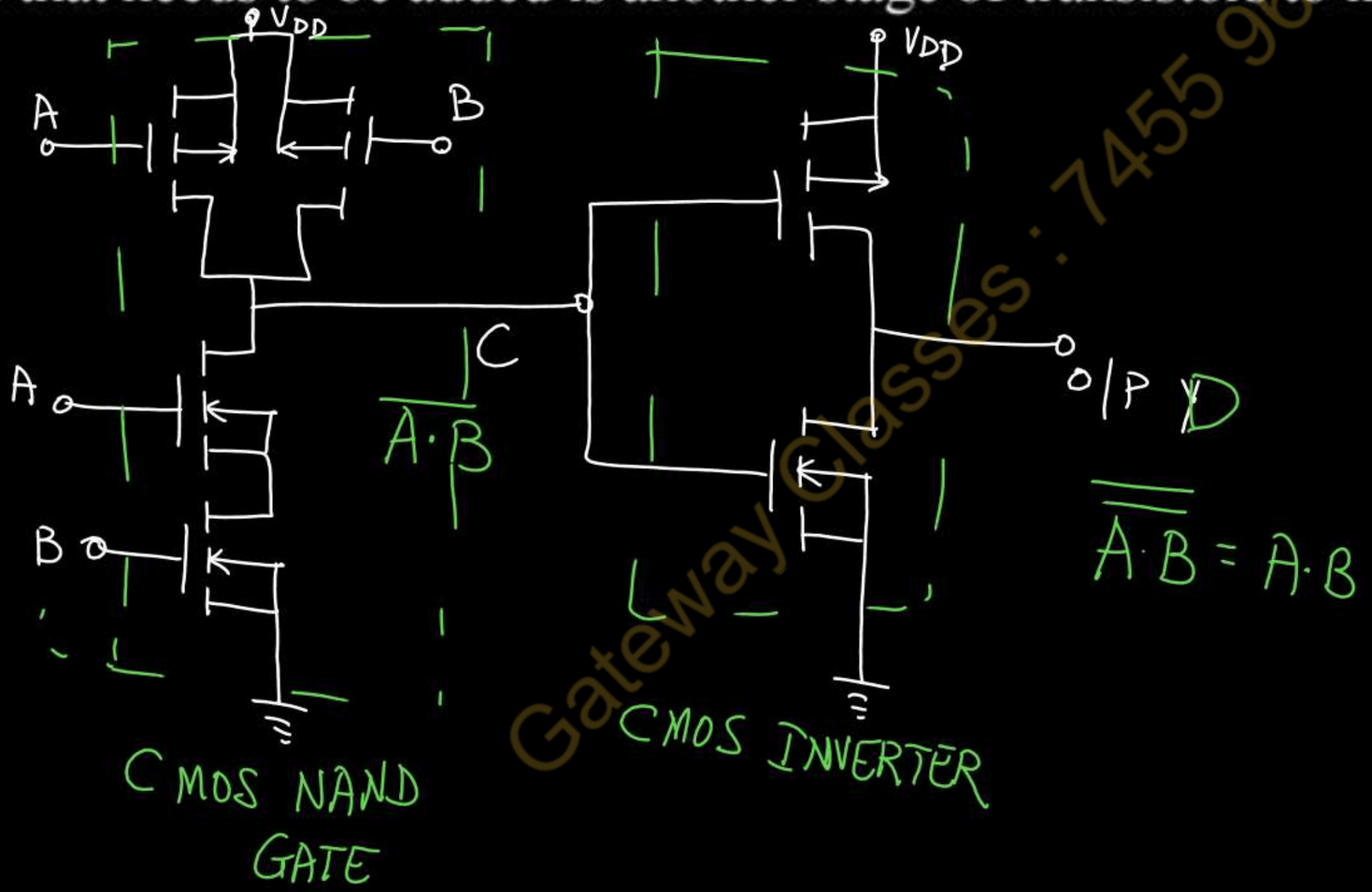
A	B	G_1	G_2	G_3	G_4
0	0	ON	ON	OFF	OFF
0	1	ON	OFF	OFF	ON
1	0	OFF	ON	ON	OFF
1	1	OFF	OFF	ON	ON

A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Gateway Classes: 7455961284

CMOS AND Gate

- CMOS NAND gate circuit may be used as the starting point for the creation of an AND gate.
- All that needs to be added is another stage of transistors to invert the output signal.



$\overline{A \cdot B} = A \cdot B$

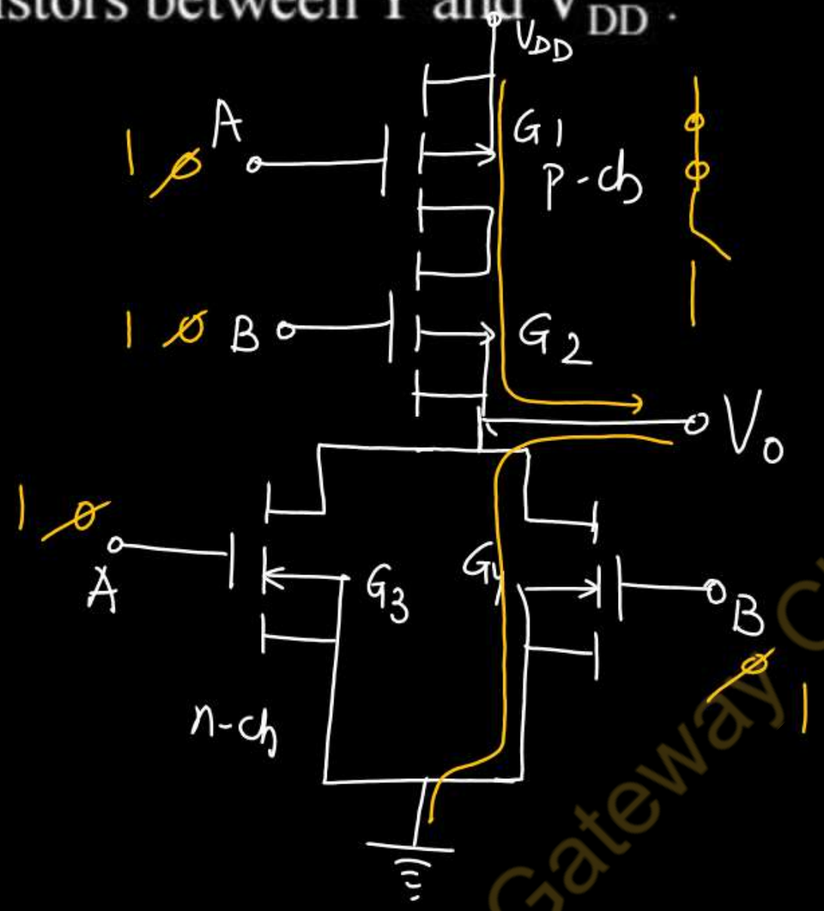
AND

A	B	C	D
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

Gateway Classes : 7455 9612 84

CMOS NOR Gate

- It consists of two paralle NMOS transistors between Y and Ground and two series PMOS transistors between Y and V_{DD} .



G_1	G_2	G_3	G_4
ON	ON	OFF	OFF
ON	OFF	OFF	ON
OFF	ON	ON	OFF
OFF	OFF	ON	ON

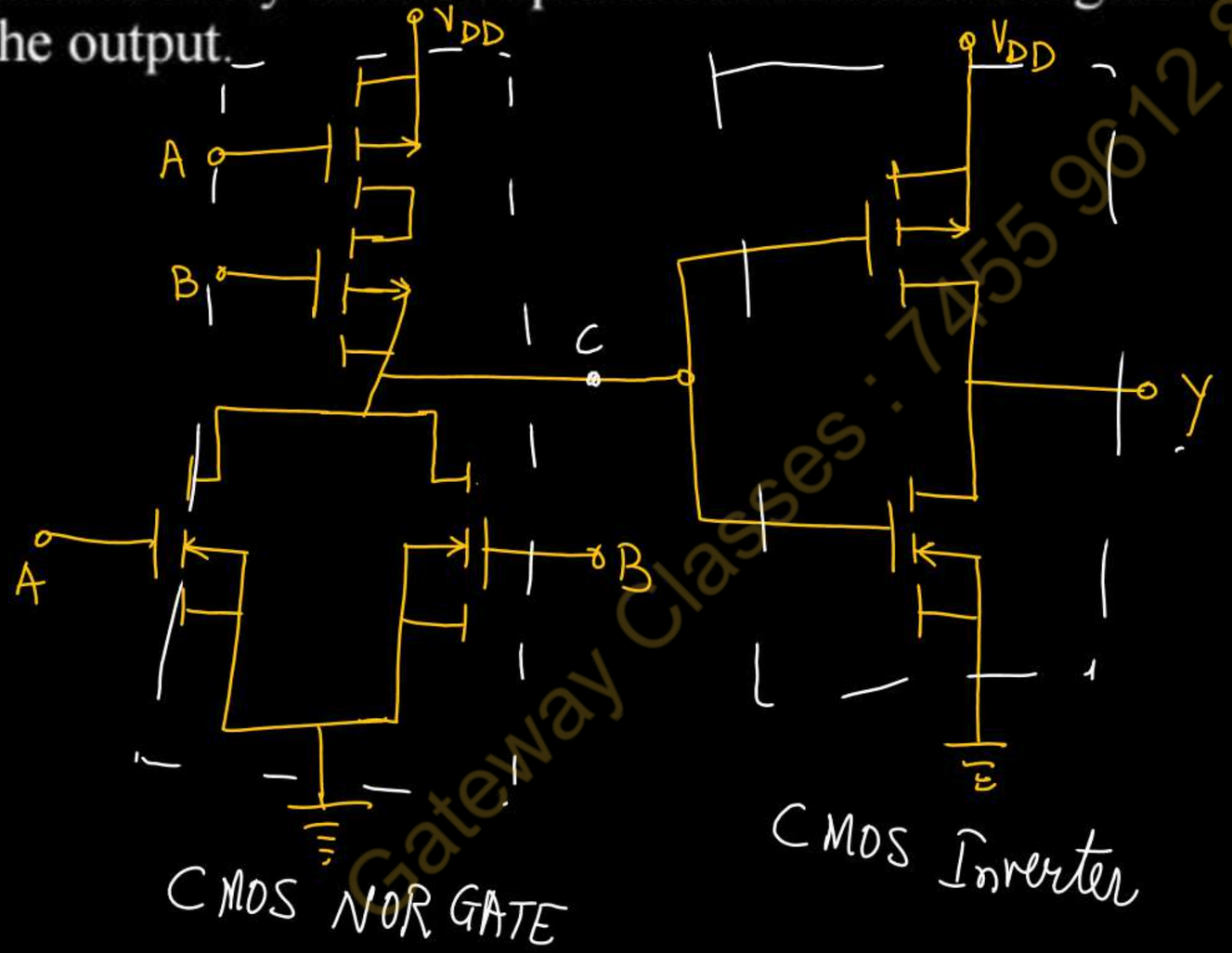
A	B	Output Y
0	0	1
0	1	0
1	0	0
1	1	0

$\overline{A+B}$

Gateway Classes : 7455 9612 84

CMOS OR Gate

- The OR function may be built up from the basic NOR gate with the addition of an inverter stage on the output.



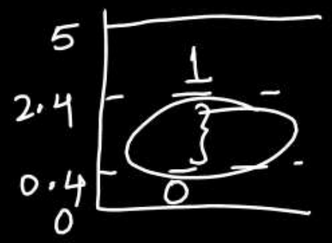
C	A	B	Output Y
1	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1

$\overline{A+B}$ $\overline{\overline{A+B}} = A+B$

Gateway Classes : 7455 9012 84

Noise Immunity of TTL & CMOS ICs

- Digital logic requires specific voltages to be recognized as L or H.
  TTL voltage levels at 5V are:
- L - max 0.4V ✓
- H - min 2.4V



- CMOS at 5V requires:
- L - max 1.5V
- H - min 3.5V
- TTL on current side has better characteristics cause input currents are much higher:
- L - -1.6 mA ✓
- H - 40 uA ✓
- CMOS has very low input current in range of 100nA, 0.1uA.
- If input voltage is in-between then there is no guaranty which level will be recognized and logic gate might oscillate. In CMOS case both transistors might conduct what will increase power consumption. This also happens in case of slow slew rate input signal (current per pin is in range of few mA).

Gateway Classes : 7455 9612 84

Figure of Merit

- The figure of merit of a digital IC is defined as the product of speed and power.
- The speed is specified in terms of propagation delay time expressed in nanoseconds.
- Figure of merit = propagation delay time (ns) x power (mW)
- It is specified in pico joules (ns x mW = pJ)

Gateway Classes : 7455961284

Specifications	TTL	CMOS
Basic Gate	NAND	NOR/NAND
Components	Passive Elements & Transistors	MOSFETs
Fan-out	10	>50
Noise Immunity	Strong	Extremely Strong
Noise Margin	Moderate	High
TPD in ns	1.5 to 30	1 to 210
Clock Rate in MHz	35	10
Power/Gate in mWatt	10	0.0025
Figure of Merit	100	0.7

Gateway Classes: 7455 9612 84

UNIVERSITY QUESTIONS

YEAR	QUESTIONS	MARKS
22-23 19-20	Define PLD's. Implement the following function using PLA $F1 = \Sigma m(0,3,4,7)$ $F2 = \Sigma m(1,2,5,7)$	10 Marks
18-19	Differentiate between PLA and PAL. Realize the full adder circuit using PAL.	7 Marks
18-19	Tabulate the truth table for 8x4 ROM that implements the Boolean function: $A(x, y, z) = \sum(1, 2, 4, 6)$ $B(x, y, z) = \sum(0, 1, 6, 7)$ $C(x, y, Z) = \sum(2, 6)$ $D(x, y, z) = \sum(1, 2, 3, 5, 7)$	7 Marks

Gateway Classes : 7455 961 284

Programmable Logic Devices (PLDs)

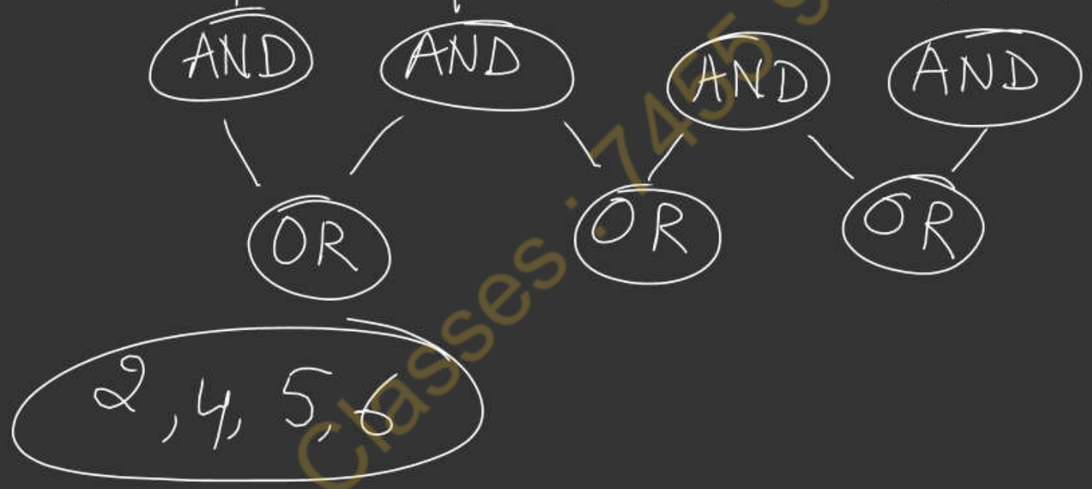
- An IC that contains large numbers of gates, flip-flops, etc. that can be configured by the user to perform different functions is called a Programmable Logic Device (PLD).
- The internal logic gates and/or connections of PLDs can be changed/configured by a programming process.
- One of the simplest programming technologies is to use fuses.
- In the original state of the device, all the fuses are intact.
- Programming the device involves blowing those fuses along the paths that must be removed in order to obtain the particular configuration of the desired logic function.
- PLDs are typically built with an array of AND gates (AND-array) and an array of OR gates (OR-array).



Gateway Classes : 1455 9612 84

SOP: $Y = \sum m(0, 1, 3, 7)$

$= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}BC + ABC$



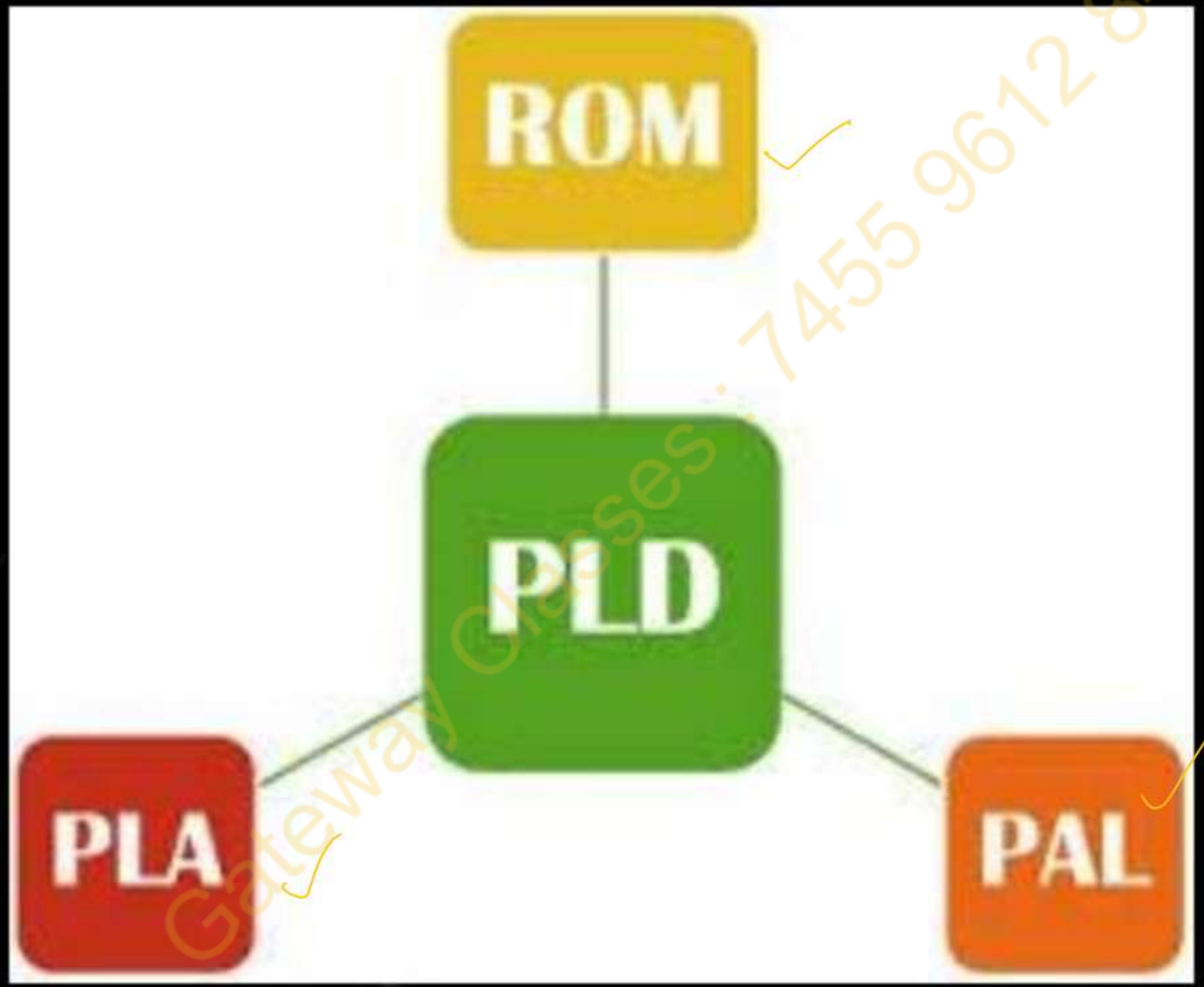
Gateway Classes 7455 961284

Advantages of using PLDs:

Problems of using standard ICs:	Advantages of using PLDs:
they require hundreds or thousands of these Ics	lower power requirements (i.e., smaller power supplies)
considerable amount of circuit board space	less board space
a great deal of time and cost in inserting, soldering, and testing.	faster
Also require keeping a significant inventory of ICs.	less costly assembly processes
	higher reliability (fewer ICs and circuit connections means easier troubleshooting)
	availability of design software.

Gateway Classes : 7405 961284

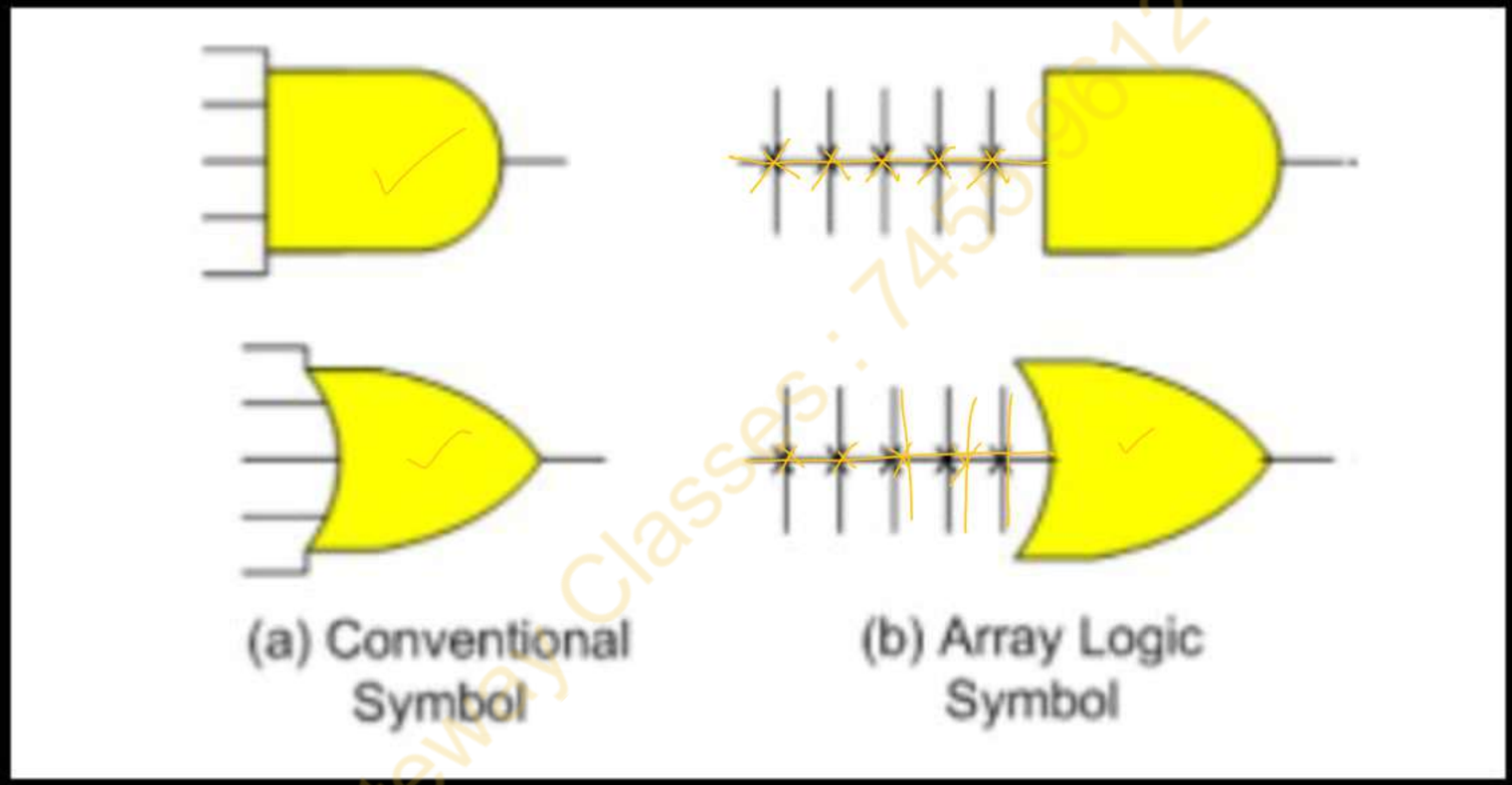
Three fundamental types of standard PLDs



Gateway Classes : 7455 9612 84

Conventional and Array Logic Symbols



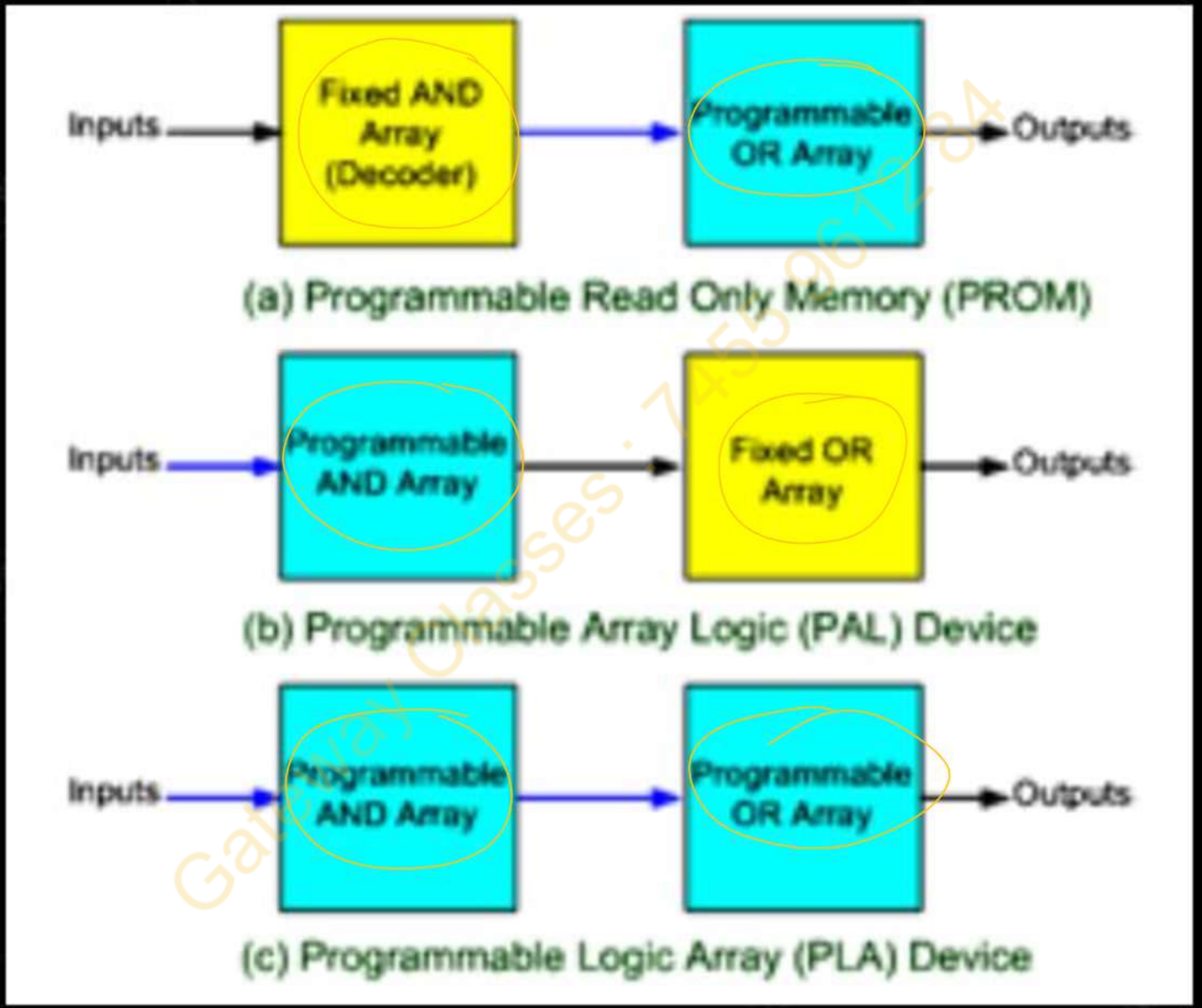


Gateway Classes : 7455 96 12 84

Three Fundamental Types of PLDs:

- The PROM (Programmable Read Only Memory) has a fixed AND array (constructed as a decoder) and programmable connections for the output OR gates array. The PROM implements Boolean functions in sum-of-minterms form.
- The PAL (Programmable Array Logic) device has a programmable AND array and fixed connections for the OR array.
- The PLA (Programmable Logic Array) has programmable connections for both AND and OR arrays. So it is the most flexible type of PLD.

Gateway Classes .7455 961284

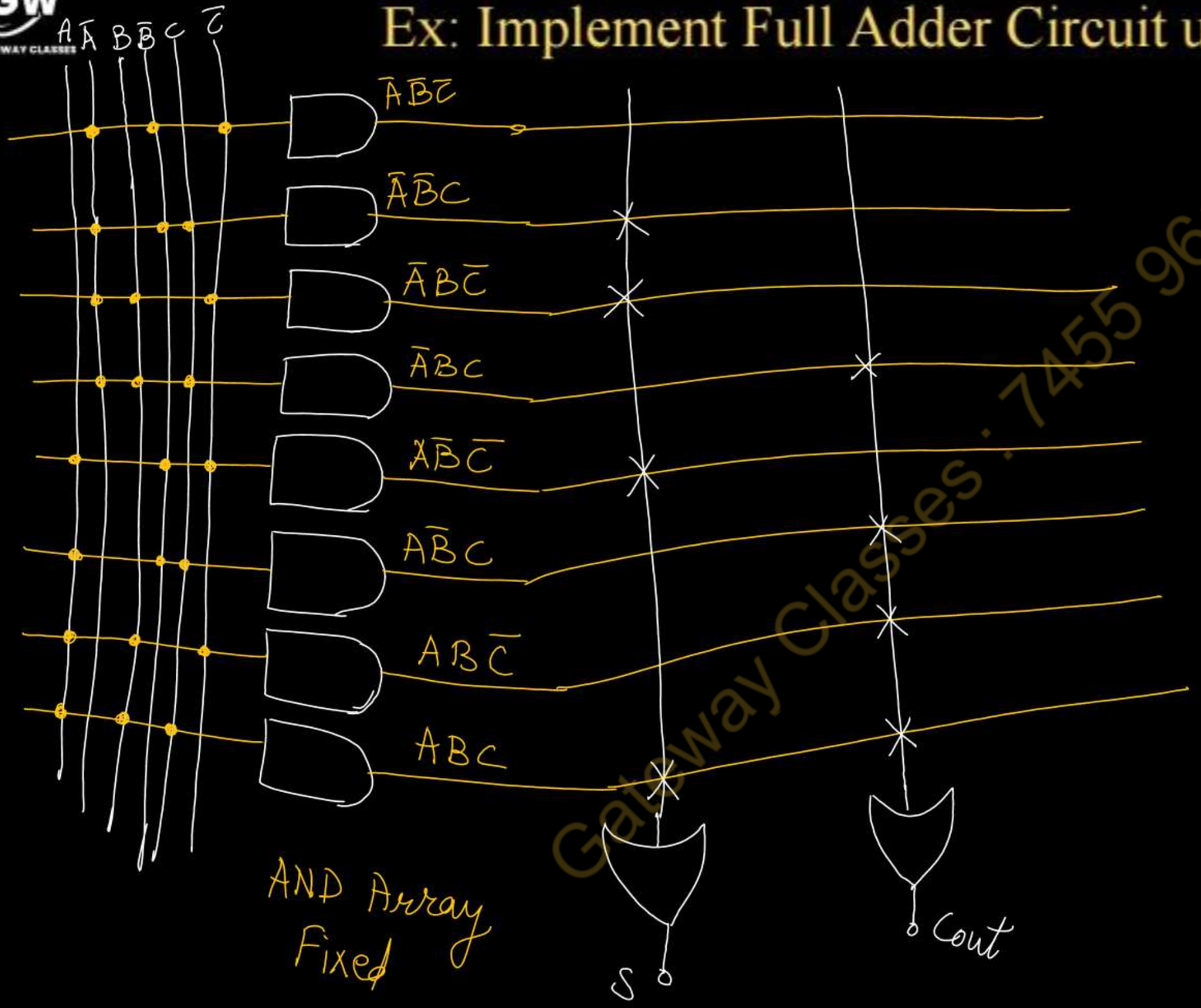

Inputs
Fixed AND Array (Decoder)
Programmable OR Array
Outputs
(a) Programmable Read Only Memory (PROM)
Inputs
Programmable AND Array
Fixed OR Array
Outputs
(b) Programmable Array Logic (PAL) Device
Inputs
Programmable AND Array
Programmable OR Array
Outputs
(c) Programmable Logic Array (PLA) Device

The ROM (Read Only Memory) or PROM (Programmable Read Only Memory):

- The input lines to the AND array are hard-wired
- the output lines to the OR array are programmable.
- Each AND gate generates one of the possible AND products (i.e., minterms).

Gateway Classes 7455 9612 84

Ex: Implement Full Adder Circuit using PROM.



A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$S = \Sigma m(1, 2, 4, 7)$

$Cout = \Sigma m(3, 5, 6, 7)$

Gateway Classes : 7455 9612 84

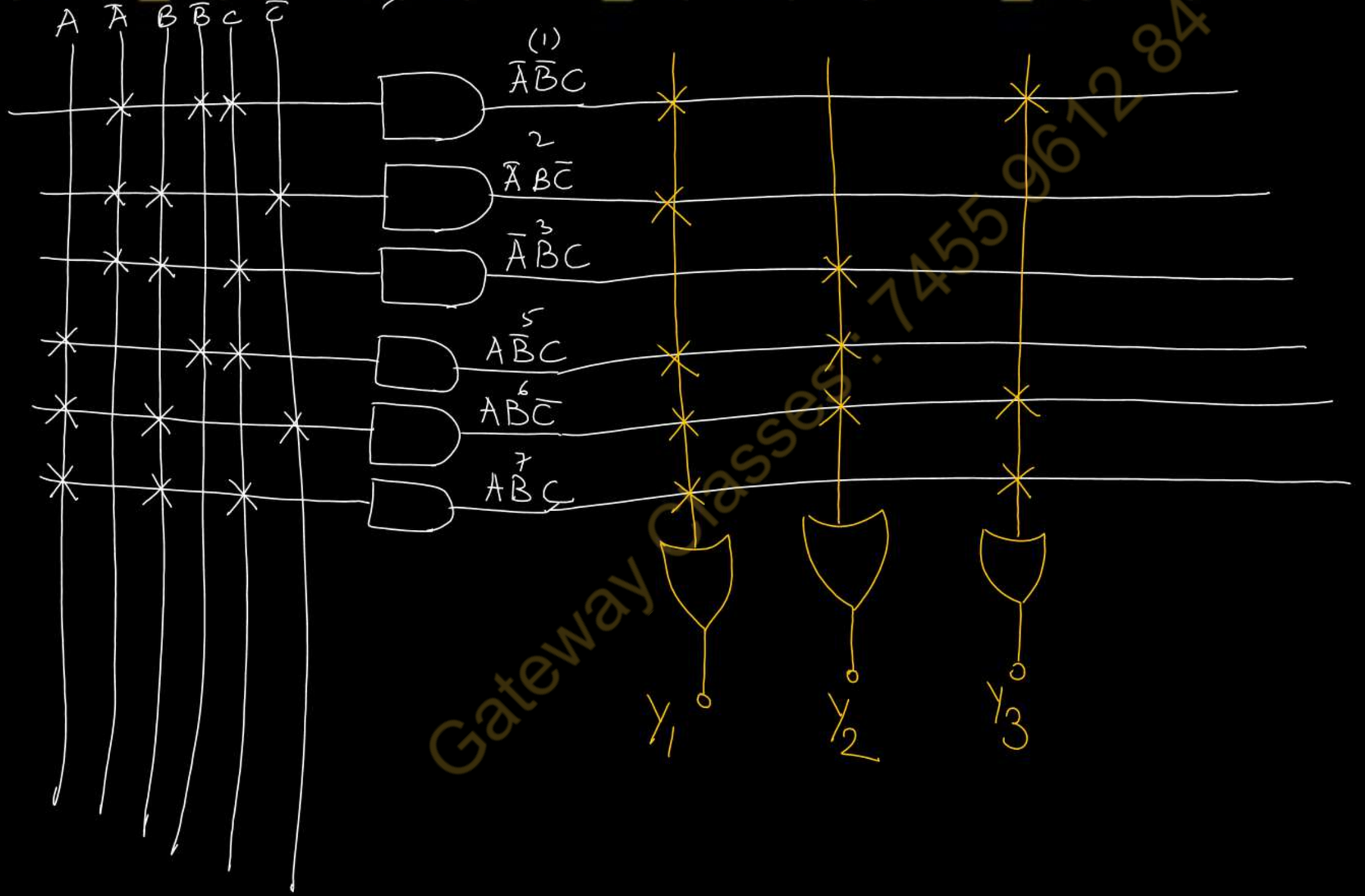
The PLA (Programmable Logic Array):

- Each of the AND gates can be programmed to generate a product term of the input variables and does not generate all the minterms as in the ROM.
- The AND and OR gates inside the PLA are initially fabricated with the links (fuses) among them.
- It consists of n inputs, m outputs, and k product terms.
- The product terms constitute a group of k AND gates each of 2n inputs.
- Links are inserted between all n inputs and their complement values to each of the AND gates.
- Links are also provided between the outputs of the AND gates and the inputs of the OR gates.
- PLA has m-outputs, the number of OR gates is m.

Gateway Classes : 7455 962 364

Ex: Implement the following boolean function using PLA:

a) $Y1 = \sum m(1,2,5,6,7)$ b) $Y2 = \sum m(3,5,6)$ c) $Y3 = \sum m(1,6,7)$



Gateway Classes: 7455 9612 84

The PAL (Programmable Array Logic):

- The PAL device is a PLD with a fixed OR array and a programmable AND array.
- PAL device is easier to program but it is not as flexible as the PLA.

Gateway Classes : 7455 961284

Example: Implement the following Boolean functions using the PAL device

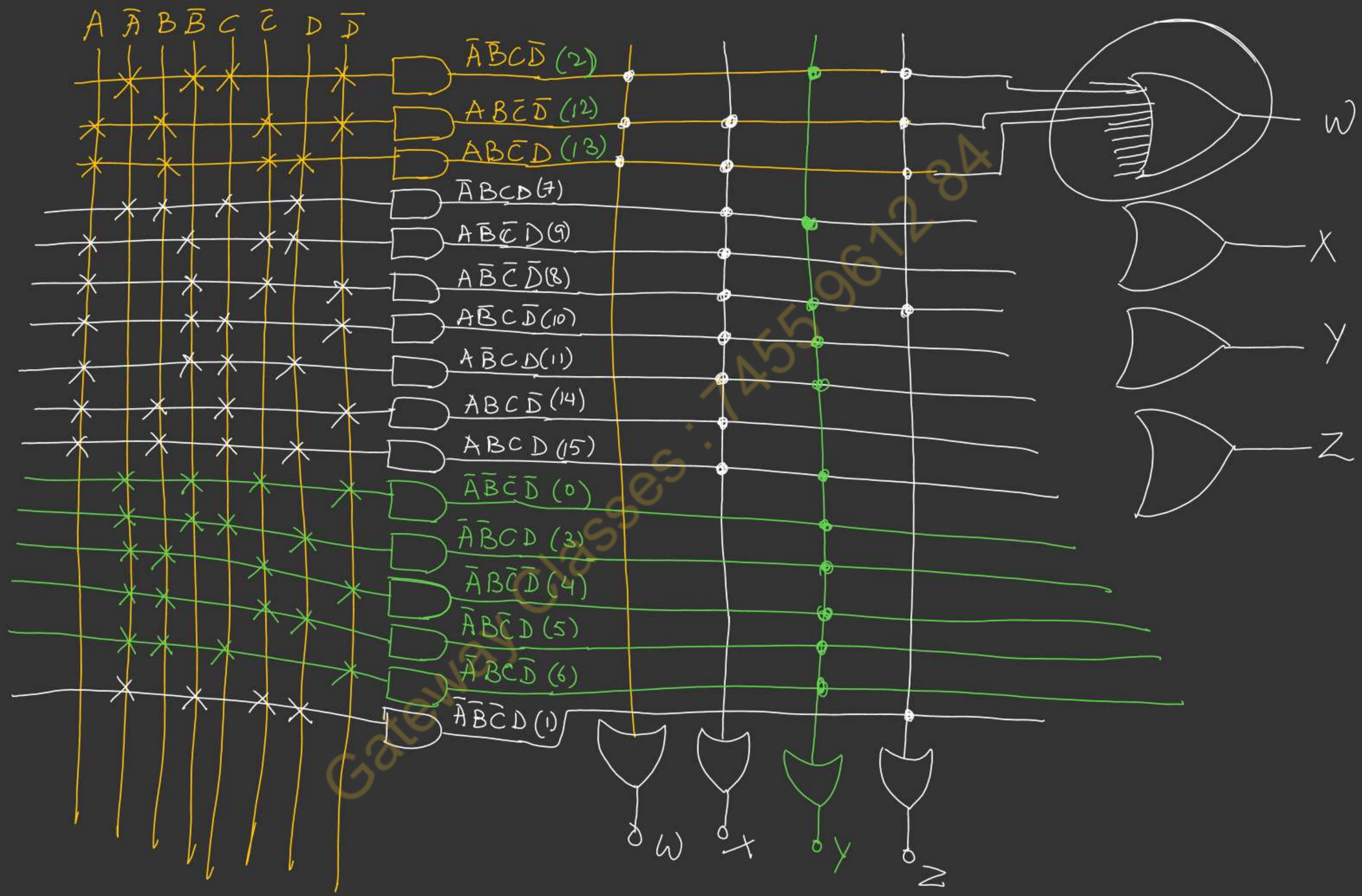
$W(A, B, C, D) = \sum m(2, 12, 13)$

$X(A, B, C, D) = \sum m(7, 8, 9, 10, 11, 12, 13, 14, 15)$

$Y(A, B, C, D) = \sum m(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)$

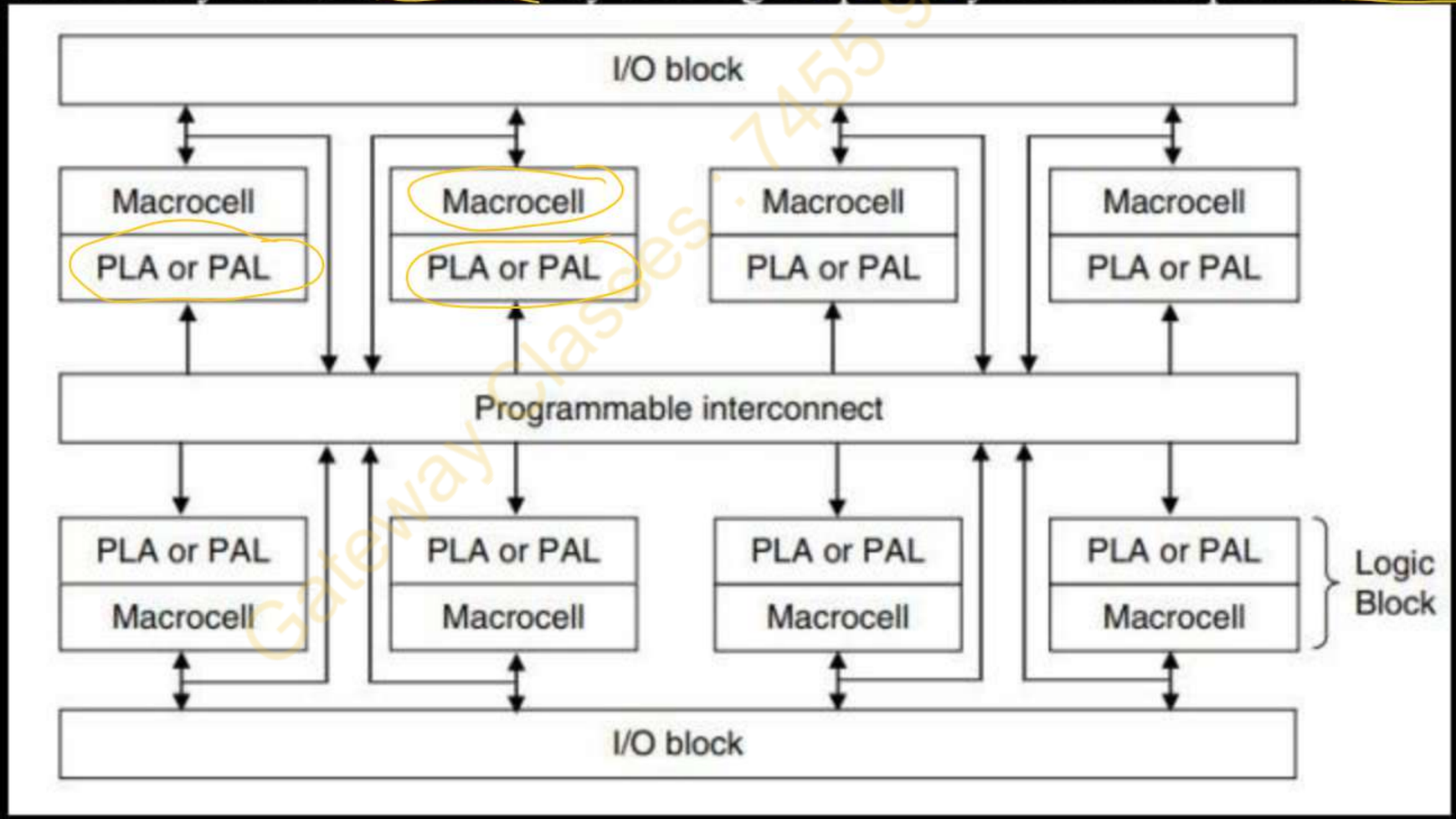
$Z(A, B, C, D) = \sum m(1, 2, 8, 12, 13)$

Gateway Classes : 7455 9612 84


A Ā B B̄ C C̄ D D̄
ĀB̄CD̄ (2)
AB̄C̄D̄ (12)
AB̄CD (13)
ĀBCD (7)
AB̄C̄D (9)
AB̄C̄D̄ (8)
AB̄CD̄ (10)
ĀBC̄D (11)
ABCD̄ (14)
ABCD (15)
ĀB̄C̄D̄ (0)
ĀB̄CD (3)
ĀBC̄D̄ (4)
ĀBC̄D (5)
ĀBCD̄ (6)
ĀB̄C̄D (1)
W
X
Y
Z
W
X
Y
Z
Gateway Classes : 7455961284

Complex Programmable Logic Devices (CPLDs)

- It is developed on top of PLD devices to create much larger and complex designs.
- A CPLD consists of a number logic blocks (or functional blocks), which internally consists of either a PLA or a PAL along with a Macrocell.
- Macrocell consists of any additional circuitry and signal polarity control to provide true signal or its complement.



Gateway Classes · 7455 9612 84

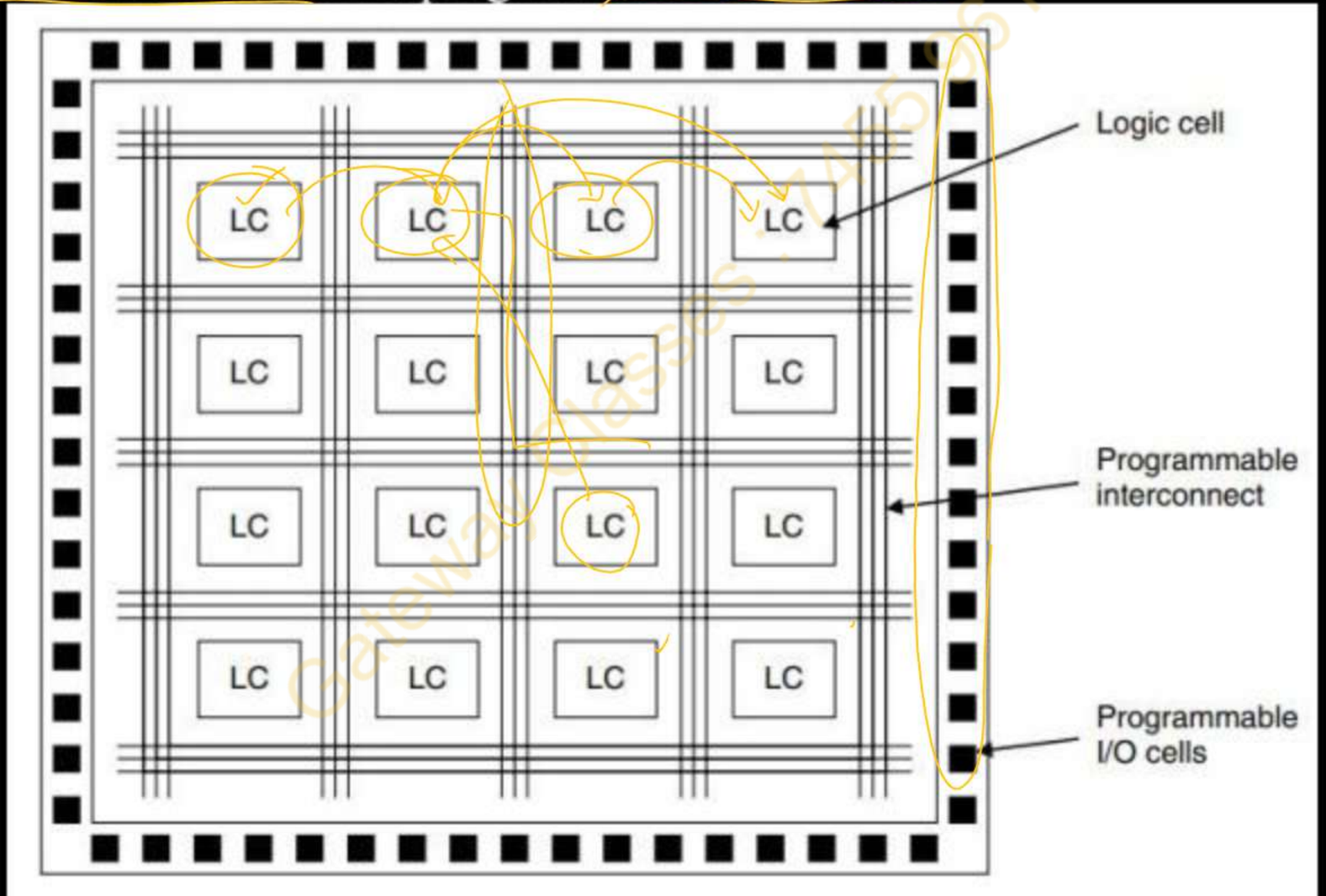
What is an FPGA?

- Field Programmable Gate Arrays or FPGAs in short are pre-fabricated Silicon devices that consists of a matrix of reconfigurable logic circuitry and programmable interconnects arranged in a two-dimensional array.
- The programmable Logic Cells can be configured to perform any digital function and the programmable interconnects (or switches) provide the connections among different logic cells.
- Using an FPGA, you can implement any custom design by specifying the logic or function of each logic block and setting the connection of each programmable switch.
- Since this process of designing a custom circuit is done in the field rather than in a fab, the device is known as “Field Programmable”.

Gateway Classes 7455 3612 04

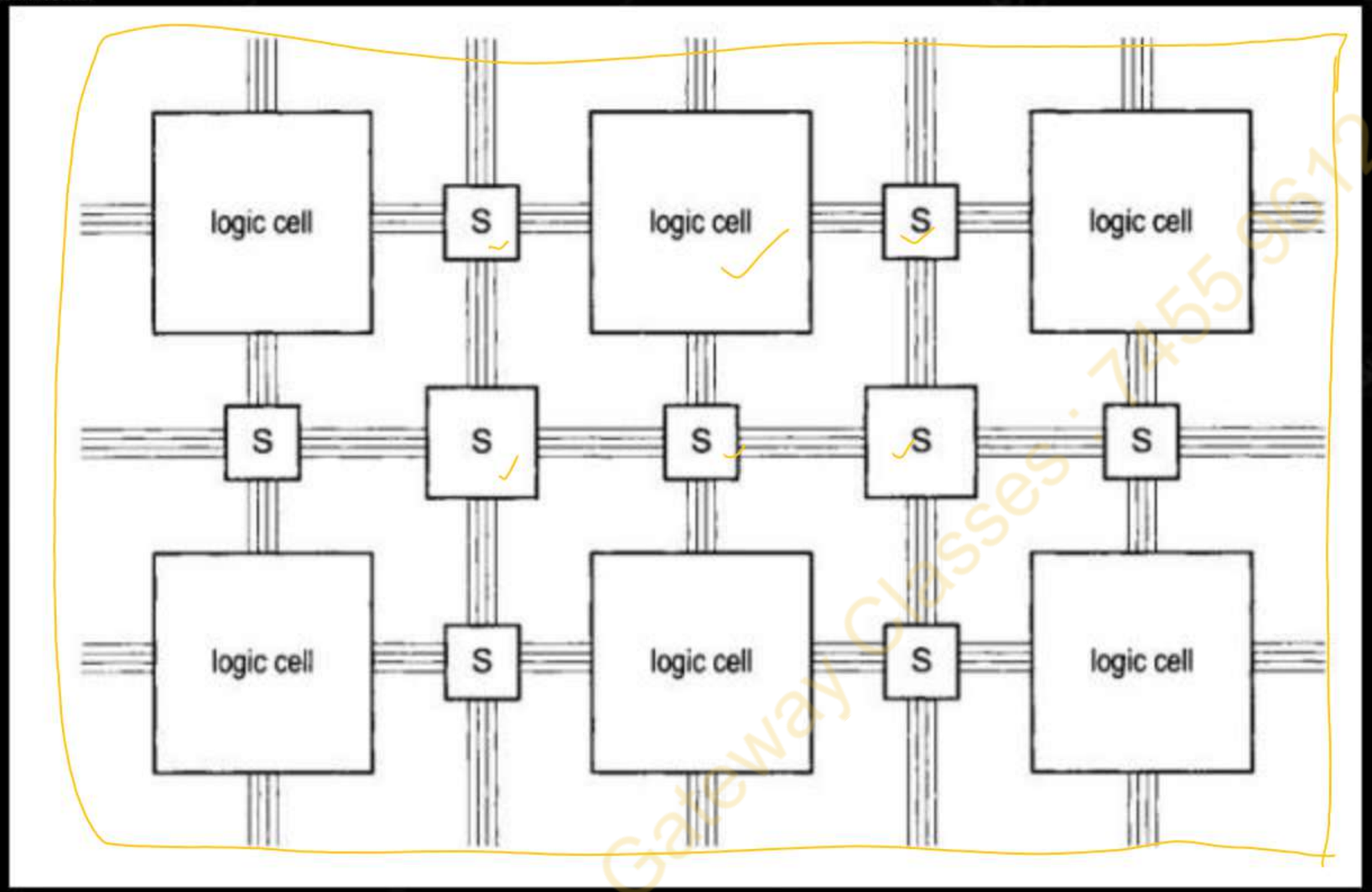
Field Programmable Gate Arrays (FPGA)

- FPGA are even more complex than CPLDs.
- The architecture of an FPGA is completely different as it consists of programmable Logic Cells, programmable interconnects and programmable IO blocks.



Gateway Classes : MAB 9612 84

Internal Structure of an FPGA



- The core of the FPGA is made up of configurable logic cells and programmable interconnections.
- These are surrounded by a number of programmable IO blocks, which are used to talk to the external world.

Gateway Classes : 7455 961284

Components of an FPGA

Typically, an FPGA consists of three basic components. They are:

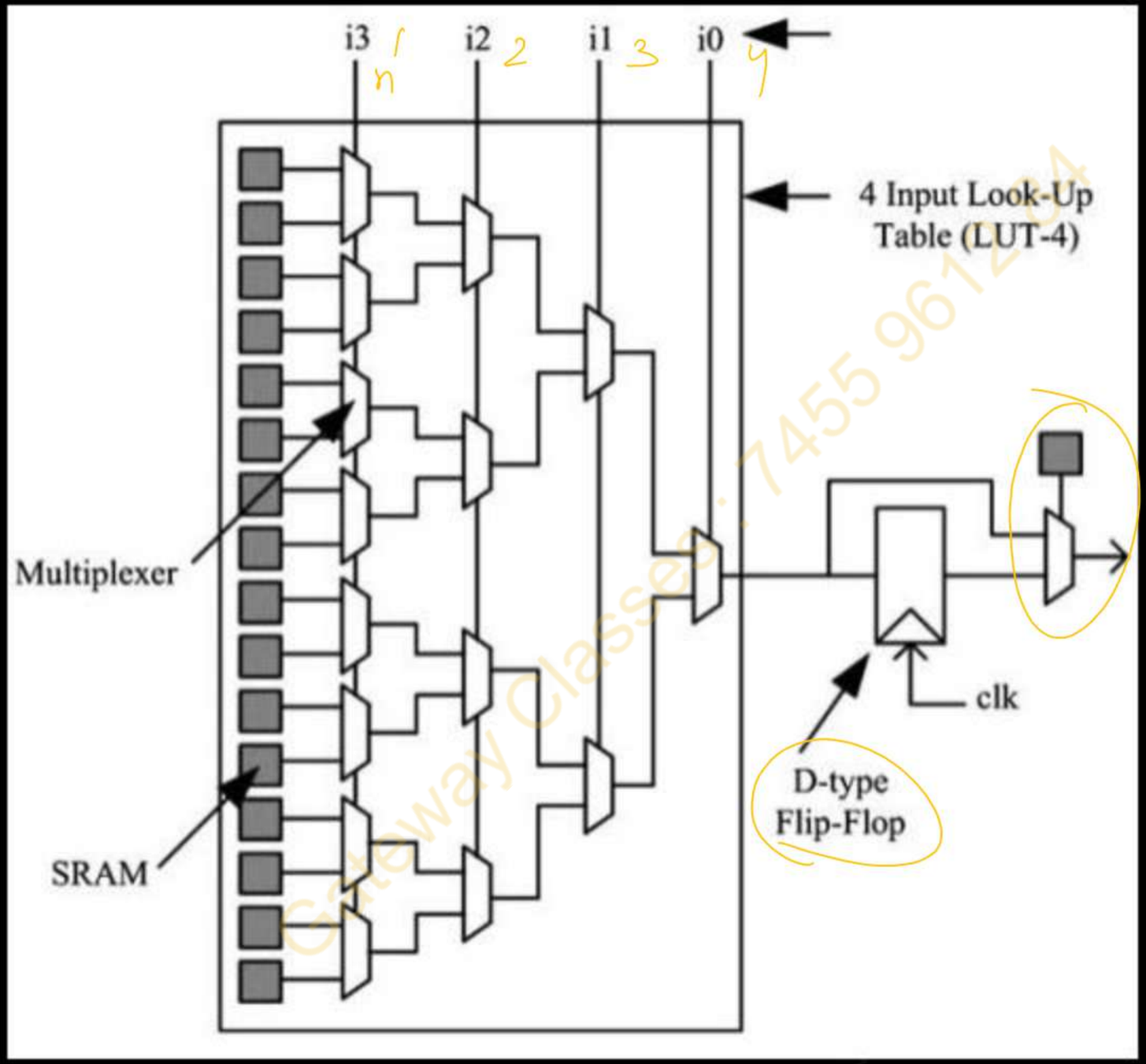
- Programmable Logic Cells (or Logic Blocks) – responsible for implementing the core logic functions.
- Programmable Routing – responsible for connecting the Logic Blocks.
- IO Blocks – which are connected to the Logic Blocks through the routing and help to make external connections.

Gateway Classes : 7455961284

Logic Block

- The Logic Block in Xilinx based FPGAs are called as Configurable Logic Blocks or CLB while the similar structures in Altera based FPGAs called Logic Array Blocks or LAB.
- A CLB is the basic component of an FPGA, which provides both the logic and storage functionalities.
- The basic logic block can be anything like a transistor, a NAND gate, Multiplexers, Look-up Table (LUT), a PAL like structure or even a processor.
- Both Xilinx and Altera use Look-up Table (LUT) based logic blocks to implement the logic as well as the storage functionalities.
- A Logic Block can be made up of a single Basic Logic Element or a set of interconnected Basic Logic Elements, where a Basic Logic Element is a combination of a Look-up table (which is in turn made up of SRAM and Multiplexers) and a Flip-flop.
- A LUT with 'n' inputs consists of 2^n configuration bits, which are implemented by SRAM Cells. Using these 2^n SRAM Bits, the LUT can be configured to implement any logical function.

Gateway Classes: 1455 96n2 84

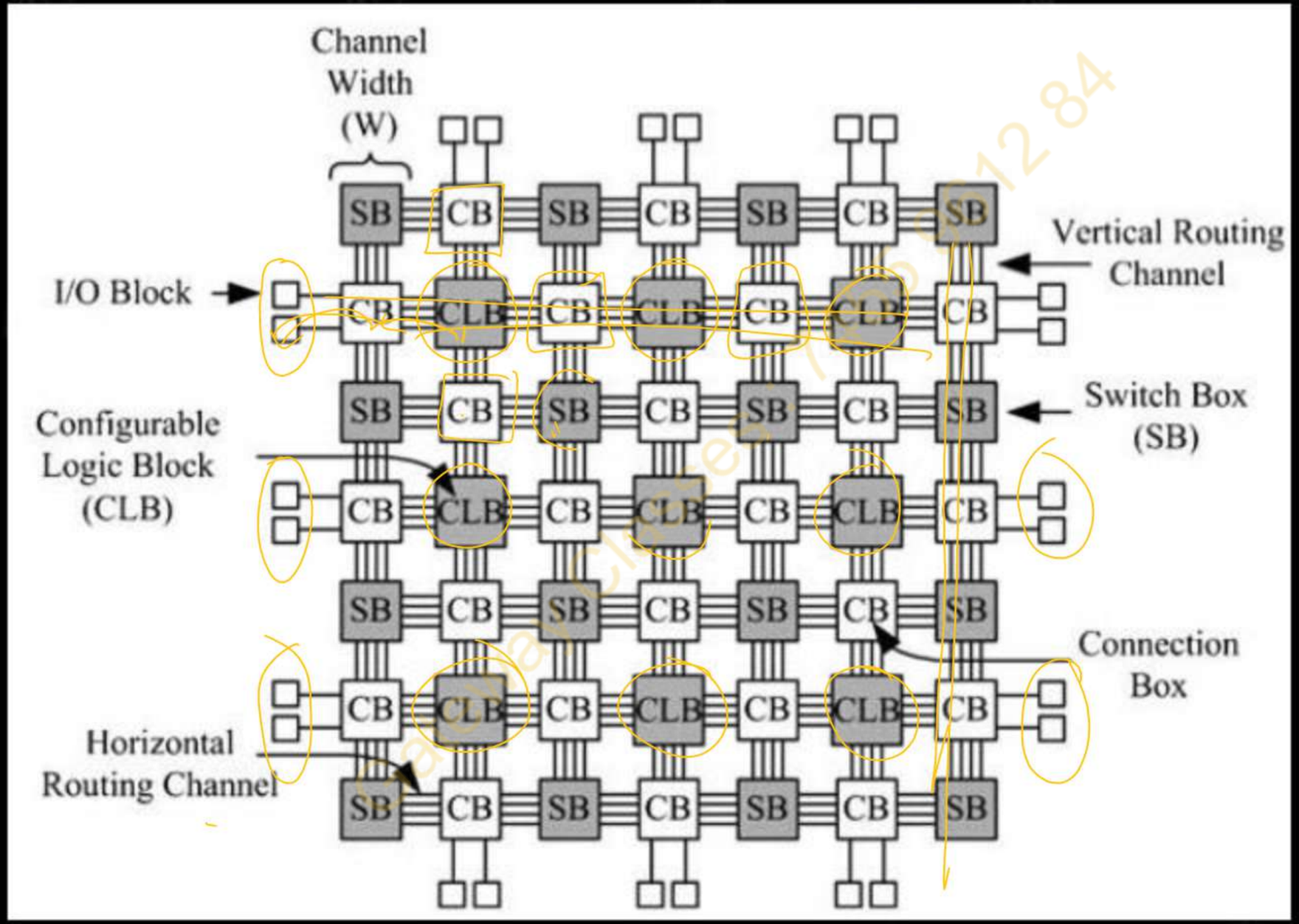

i3
i2
i1
i0
4 Input Look-Up Table (LUT-4)
Multiplexer
SRAM
clk
D-type Flip-Flop

Routing

- The programmable routing network is responsible for interconnecting these logic blocks.
- The Routing Network provides interconnections between one logic block to other as well as between the logic block and the IO Block to completely implement a custom circuit.
- Basically, the routing network consists of connecting wires with programmable switches, which can be configured using any of the programming technologies.
- There are basically two types of routing architectures. They are:
- 1) Island Style Routing (also known as Mesh Routing)
- 2) Hierarchical Routing
- In island style routing architecture, the logic blocks are arranged in a two-dimensional array and are interconnected using a programmable routing network.
- This type of routing is widely used in commercial FPGAs.

Gateway Classes : 7455 961284

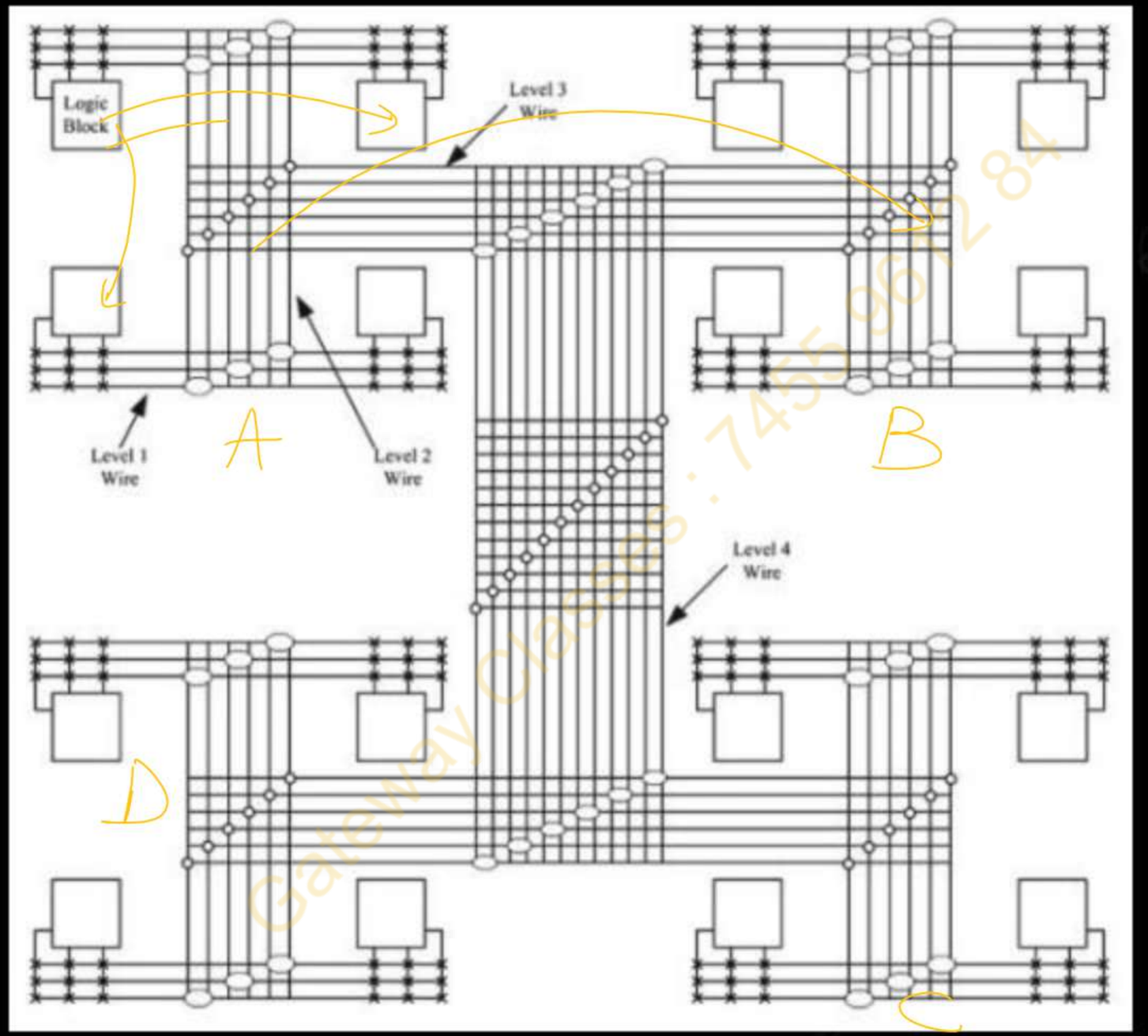
Island Style Routing



Hierarchical Routing

- Many logic blocks are confined to a local set of connections and hierarchical routing architecture makes use of this feature by dividing the logic blocks into several groups or clusters.
- If the logic blocks are residing in the same cluster, then the hierarchical routing connects them in a low level of hierarchy.
- If the logic blocks are residing in different clusters, then wiring is done over a higher level of hierarchy.

Gateway Classes : 7455 961234


Logic Block
Level 3 Wire
Level 1 Wire
A
Level 2 Wire
B
Level 4 Wire
D
C

FPGA Programming Technologies

The following are three of the well-known programming technologies used in FPGAs.

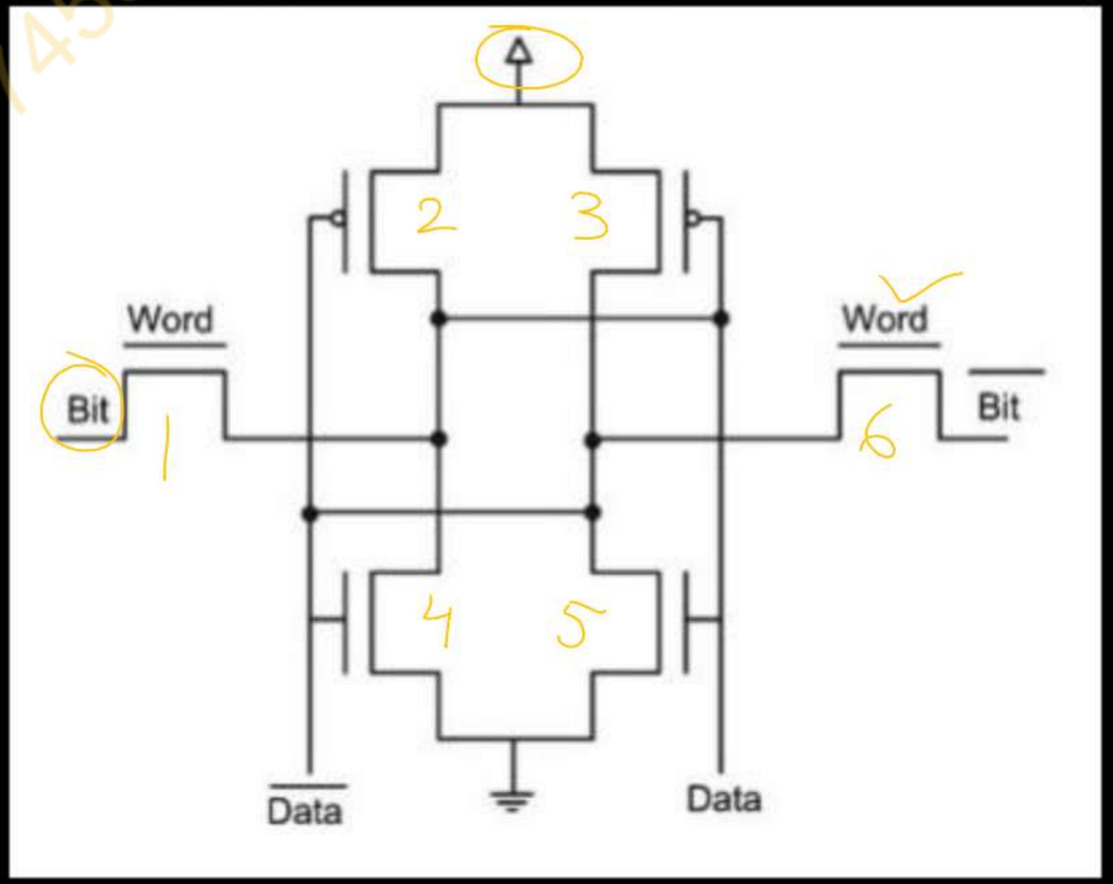
- SRAM
- EEPROM / Flash
- Anti-Fuse

Gateway Classes : 7455 961284

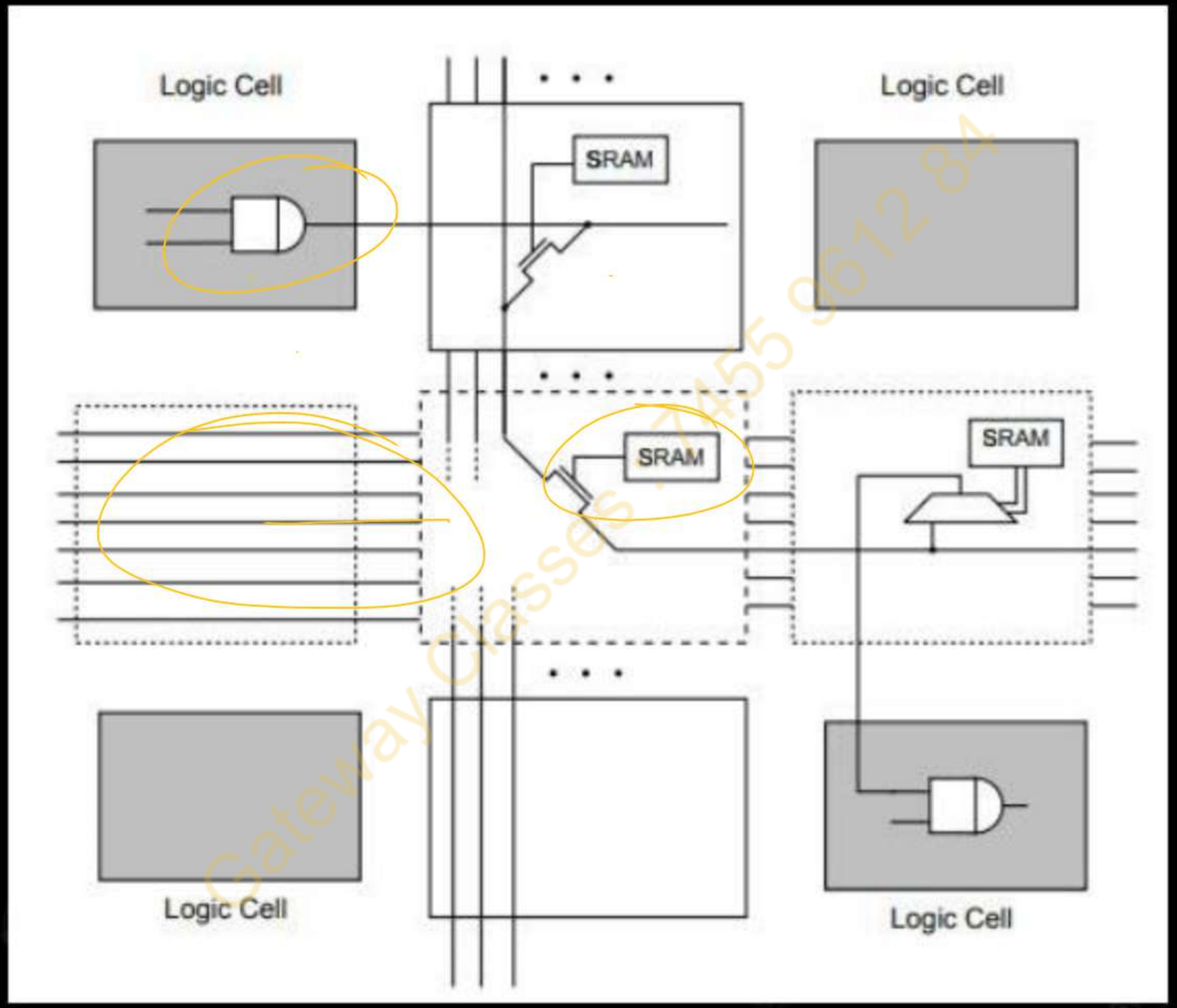
SRAM

- SRAM is short form for Static RAM.
- SRAM is designed using transistors and the term static means that the value loaded on a basic SRAM Memory Cell will remain the same until deliberately changed or when the power is removed.
- A typical 6 transistor SRAM Cell to store 1 bit is shown in the following image.

- SRAM based FPGAs are used to program both the logic cells and the interconnects and they have become quite predominant due to their re-programmability and use of CMOS technology, which is known for its low dynamic power consumption, high speed and tighter integration.



Gateway Classes : 7455 961284


Logic Cell
Logic Cell
SRAM
SRAM
SRAM
Logic Cell
Logic Cell

EEPROM / Flash

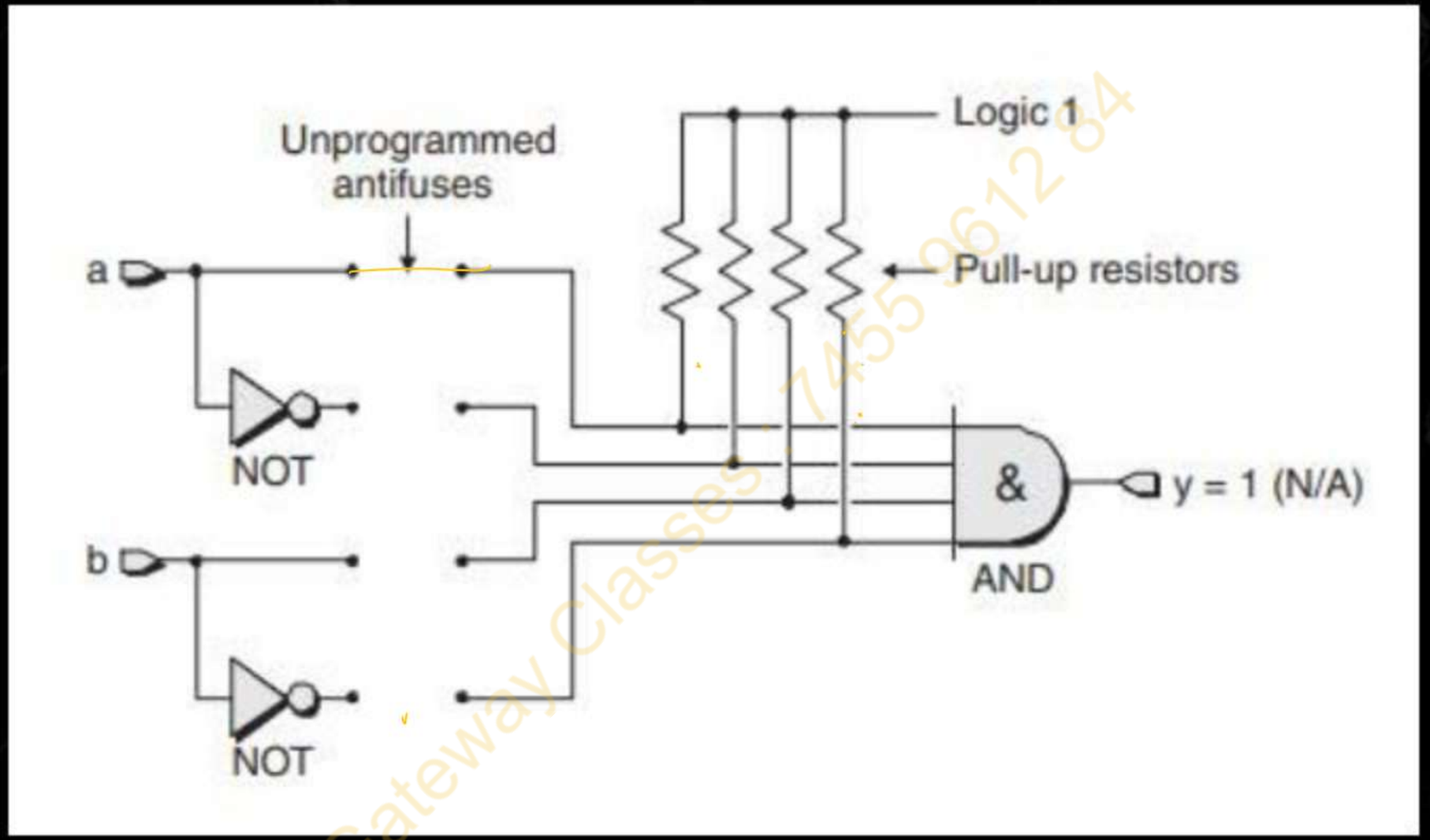
- A close alternative to SRAM based programming technology is based on EEPROM or Flash programming technologies.
- The main advantage of flash-based programming is its non-volatile nature.
- Even though flash supports re-programmability, the number of times this can be done is very small when compared to an SRAM technology.

Gateway Classes : 7455961284

Anti-Fuse

- The anti-fuse programming technology is an old technique of producing one-time programmable devices.
- They are implemented using a link called the antifuse, which in its unprogrammed state has a very high resistance and can be considered an open circuit.
- When programming, a high voltage and current is supplied to the input.
- As a result, the antifuse, which is initially in the form of amorphous silicon (basically an insulator with very high resistance) linking two metal tracks, comes to life by converting to a conducting polysilicon.
- When compared to the other two technologies, the antifuse one occupies the least amount of space but comes only as one-time programmable option.

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Applications

- Used to implement small to medium complex state machines and data processing tasks on small data.
- several automotive, consumer and industrial applications.
- An easy option to prototype ASIC designs as they can be easily reconfigured to test and try several variations of the hardware before finalizing the main design.
- implemented as direct competitors to some ASICs.
- can facilitate DSP operations
- embedded control applications
- used to implement a soft-core processor of any microcontroller along with custom IO capabilities.

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