AKTU

GATEWAY CLASSES

Digital System Design

B.Tech. 3rd Sem

EC & Allied



Exam/Result Oriented Content

- ✓ Recorded Video Lectures
- ✓ Pdf Notes
- ✓ PYQs

DIGITAL SYSTEM DESIGN

UNIT 2 : Combinational circuits

Today's Target

- Combinational circuits: steps for designing
- Half Adder
- Full Adder
- DPP
- University Questions

Combinational circuits: steps for designing

- Study required conditions
- Prepare Truth Table
- Identify Minterms and place in K-map
- Generate a reduced boolean expression.
- Realize using basic gates/ NAND gates (as required)

Example: Realize a circuit with four inputs (A,B,C,D) that provide output as logic 1 for all combination of inputs which are multiples of 3



$Y = \Sigma m(3, 6, 9, 12, 15)$

AB \ CD	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

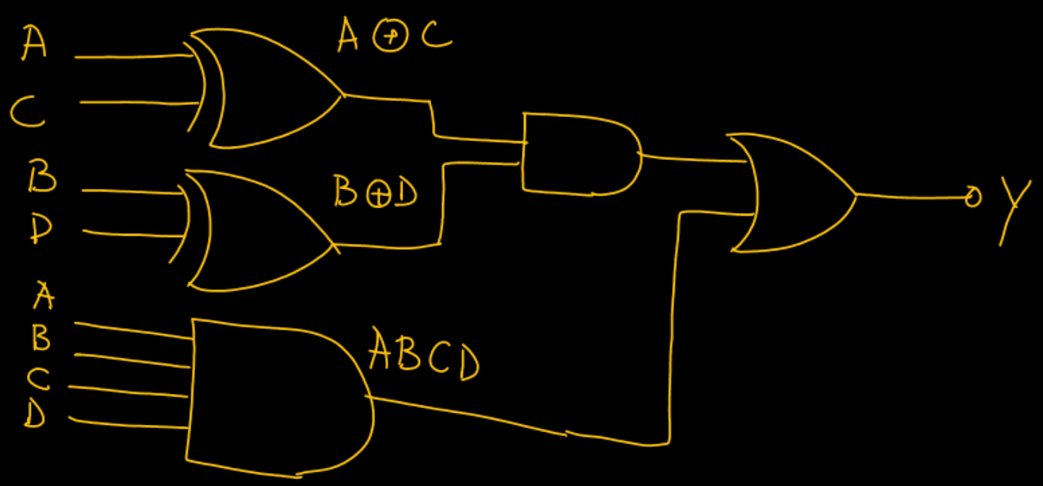
$$Y = \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}D + AB\bar{C}\bar{D} + ABCD$$

$$= \bar{B}D(\bar{A}C + A\bar{C}) + B\bar{D}(\bar{A}C + A\bar{C}) + ABCD$$

$$= \bar{B}D(A \oplus C) + B\bar{D}(A \oplus C) + ABCD$$

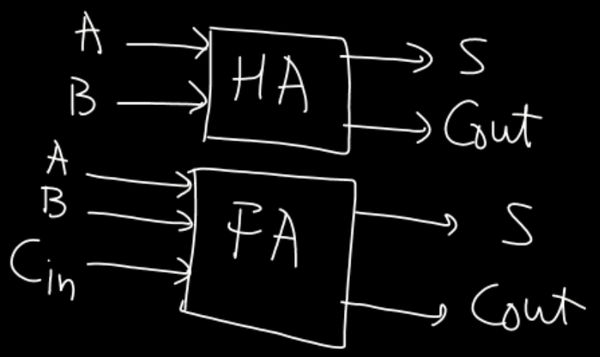
$$= (A \oplus C)(\bar{B}D + B\bar{D}) + ABCD$$

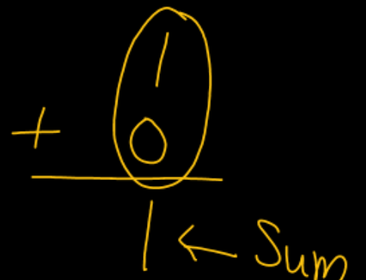
$$= (A \oplus C)(B \oplus D) + ABCD$$

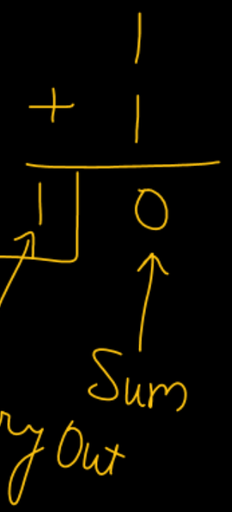


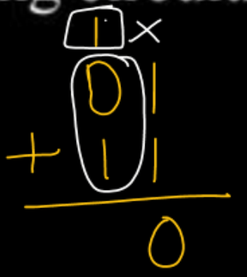
Binary Adder

- Binary Adders are arithmetic circuits in the form of half-adders and full-adders used to add together two binary digits.
- The addition of these two digits produces an output called the SUM of the addition and a second output called the CARRY or Carry-out, (C_{OUT}) bit according to the rules for binary addition.
- One of the main uses for the *Binary Adder* is in arithmetic and counting circuits.
- Binary Addition of Two Bits:
- $0 + 0 = 0$
- $0 + 1 = 1$
- $1 + 0 = 1$
- $1 + 1 = 0$ (carry = 1)

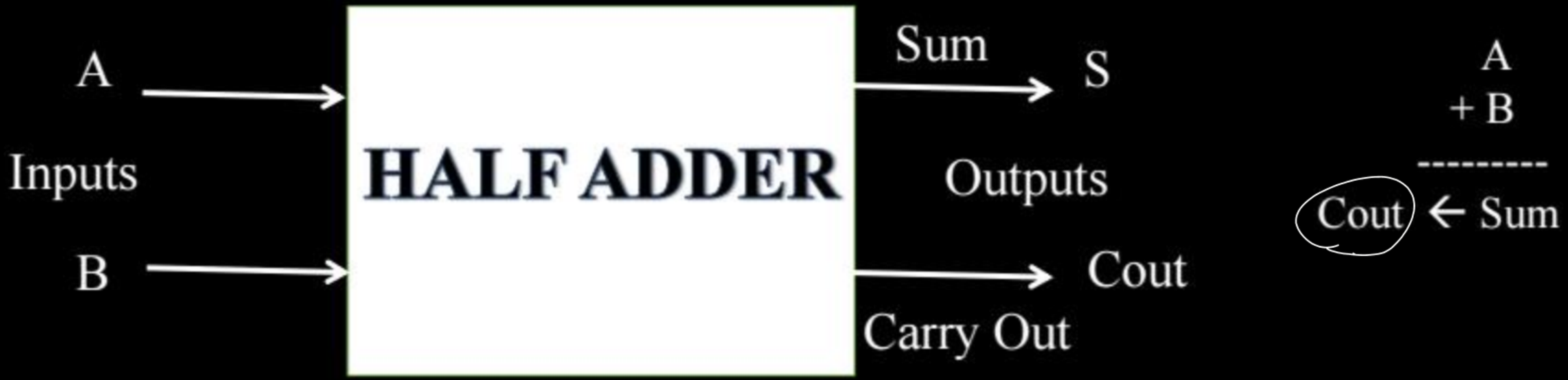








Binary Adder Block Diagram



A
+ B

Cout ← Sum

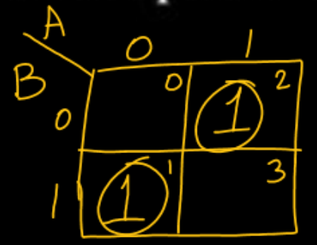
Half Adder Truth Table with Carry-Out

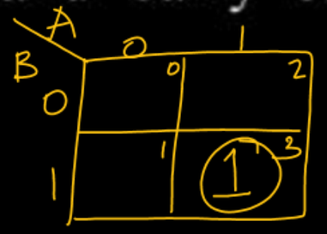
A	B	S	Cout
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$S = \Sigma m(1, 2)$

$Cout = \Sigma m(3)$

K-map for 'sum' and 'carry' & implementation using basic gates

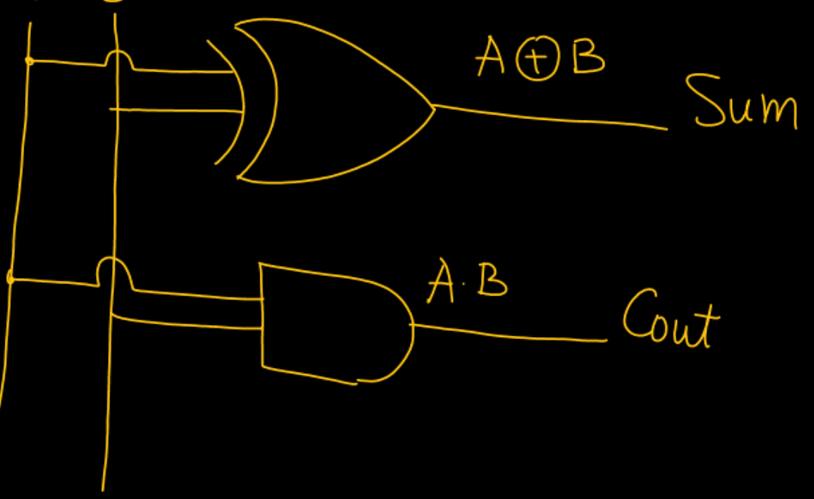


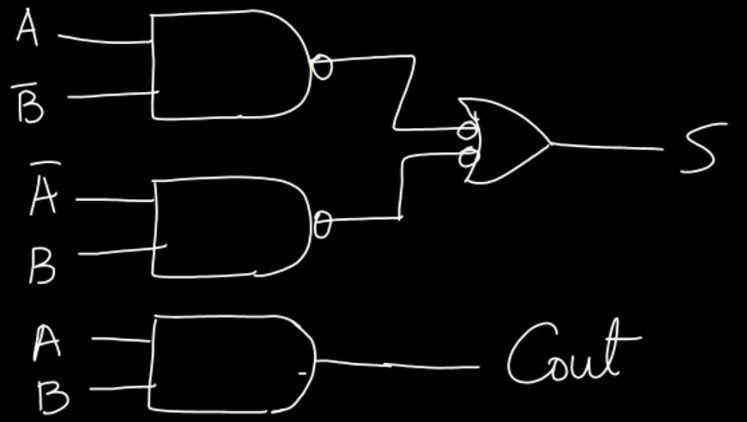


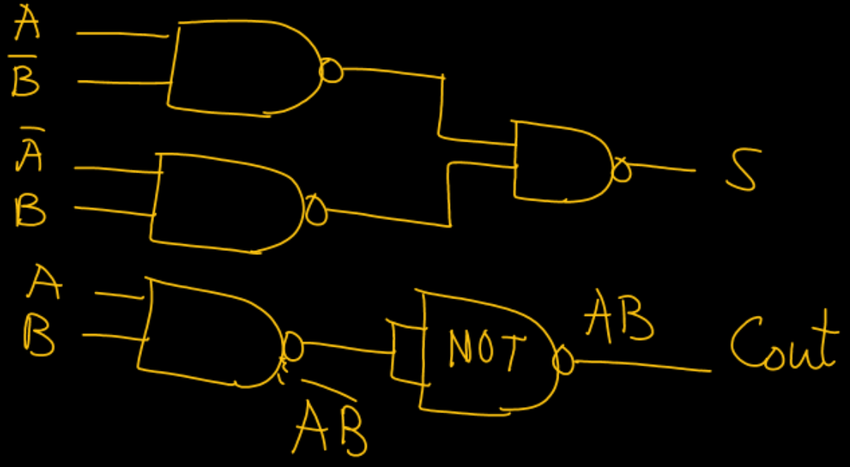
$S = A\bar{B} + \bar{A}B$ ✓

$= A \oplus B$ ×

$Cout = AB$



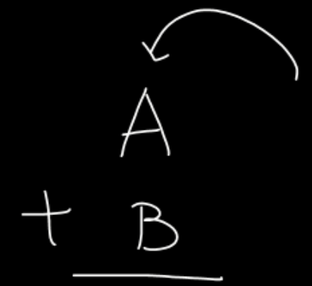




Disadvantage of the *Half Adder* circuit

- when used as a binary adder, is that there is no provision for a "Carry-in" from the previous circuit

- multiple bits of data cannot be added.



A Full Adder Circuit

- a full adder has three inputs.
- 2 bits are single bit data inputs A and B
- plus an additional *Carry-in* (C-in) input to receive the carry from a previous stage.



Cin
A
+ B

$\text{Cout} \leftarrow \overline{\text{SUM}}$

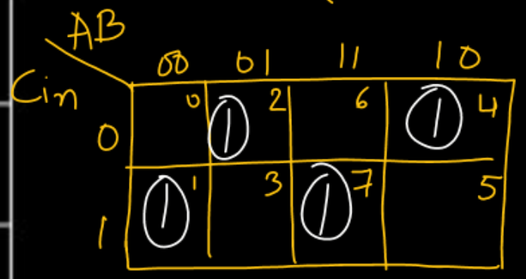
Full Adder Truth Table with Carry-Out

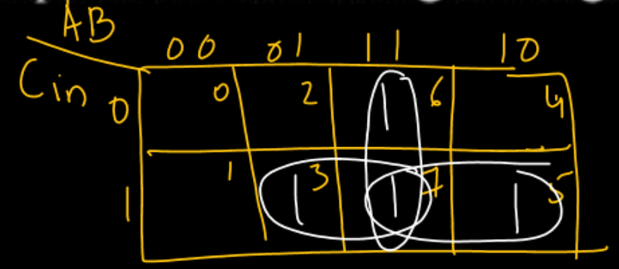
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K-map for 'sum' and 'carry' & implementation using basic gates

$S = \Sigma m(1,2,4,7)$

$Cout = \Sigma m(3,5,6,7)$





$Cout = BCin + AB + ACn$

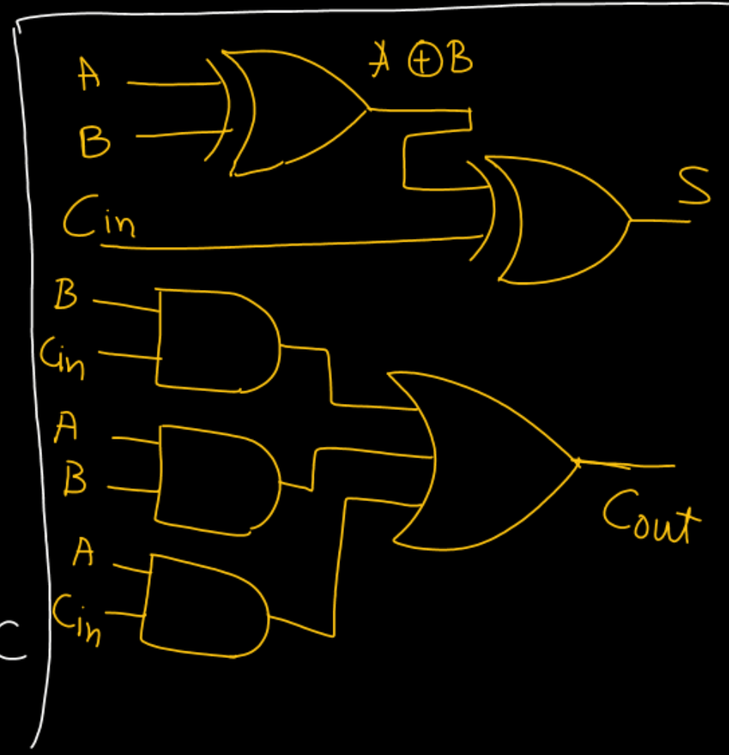
$S = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$

$= \bar{A}(B \oplus C) + A(\overline{B \oplus C})$

$B \oplus C = X$ So $\overline{B \oplus C} = \bar{X}$

$S = \bar{A}X + A\bar{X} = A \oplus X = A \oplus B \oplus C$



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a) Design Half Adder circuit using NAND gates only.

b) Design Full Adder circuit using NAND gates only.

UNIVERSITY QUESTIONS

YEAR	QUESTION	MARKS
21-22	Design a full adder by constructing the truth table and simplify the output equations.	10 marks
20-21	Construct full adder using logic gates.	2 marks

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Thank You

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