# AKTU

GATEWAY CLASSES

# Digital System Design

## B.Tech. 3rd Sem

## EC & Allied



**Exam/Result Oriented Content**

- ✓ Recorded Video Lectures
- ✓ Pdf Notes
- ✓ PYQs

# DIGITAL SYSTEM DESIGN

## UNIT 4 : Logic families and semiconductor memories

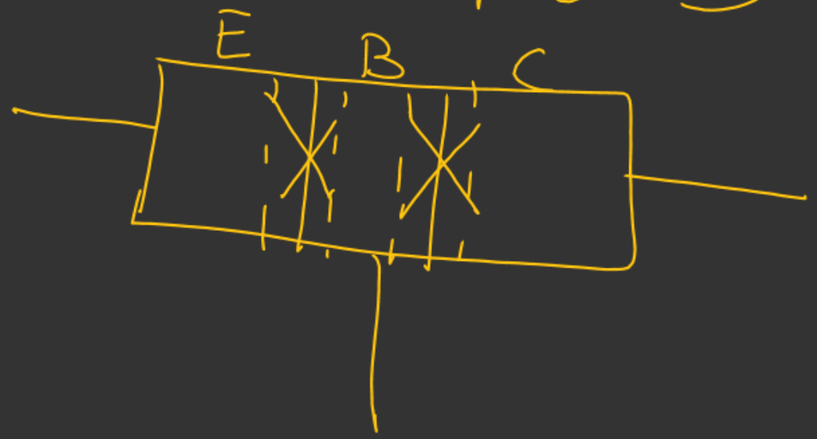
Lec 3

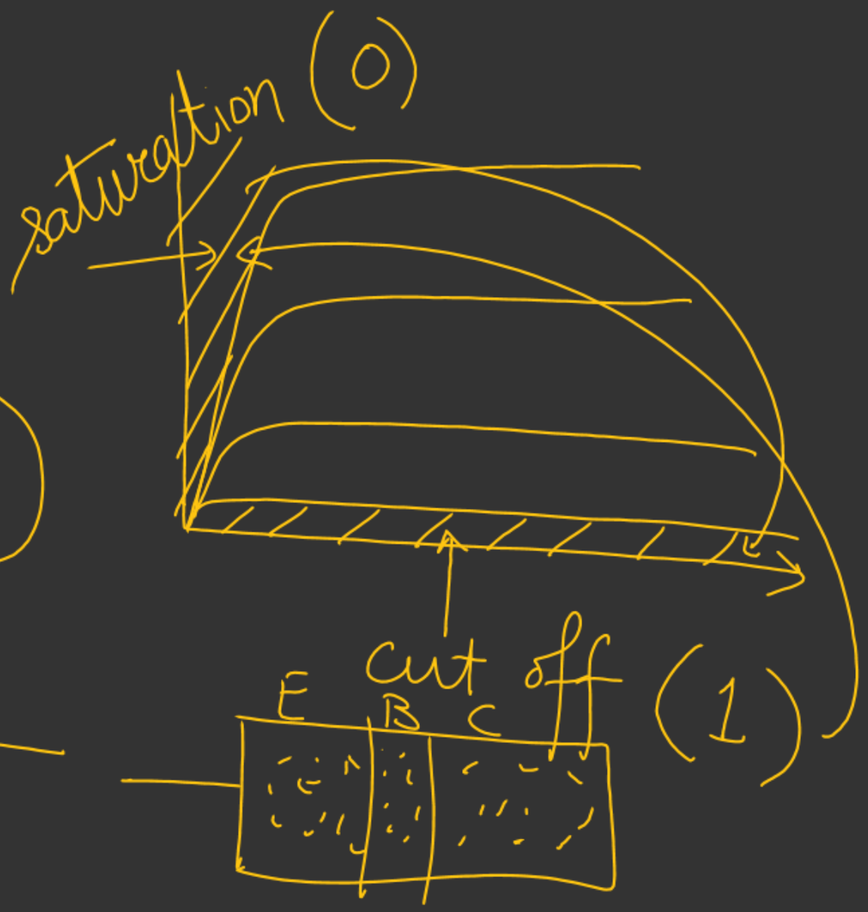
**Today's Target**

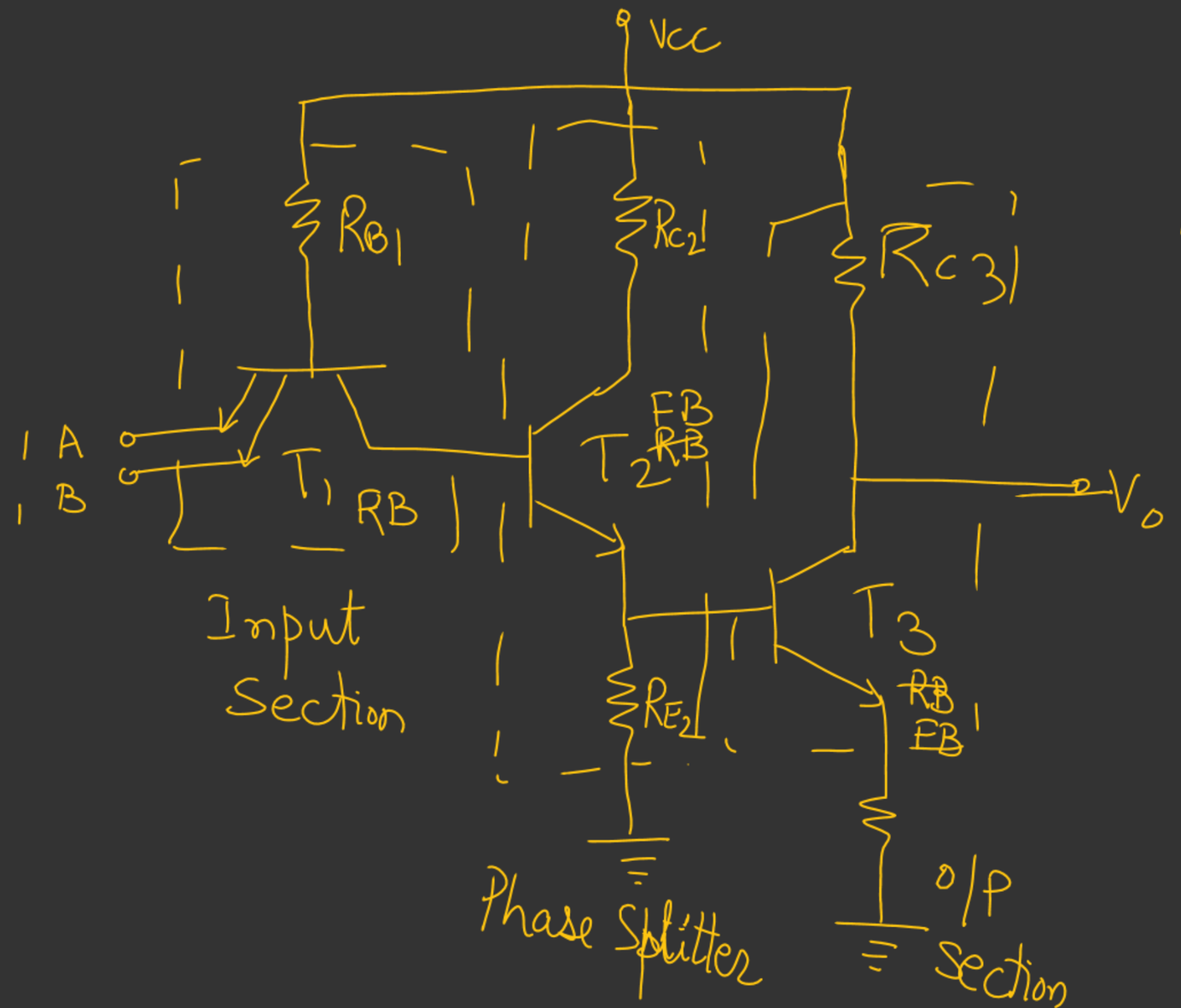
- Totem pole TTL ✓
- Totem pole TTL NOR Gate ✓
- **Three state Gate** ✓
- Schottky TTL ✓
- University Questions ✓

NAND

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |






Case 1 : I/P = 0

$V_o = 1$

$R_{C3} \Rightarrow$ low

Case 2 : I/P = 1

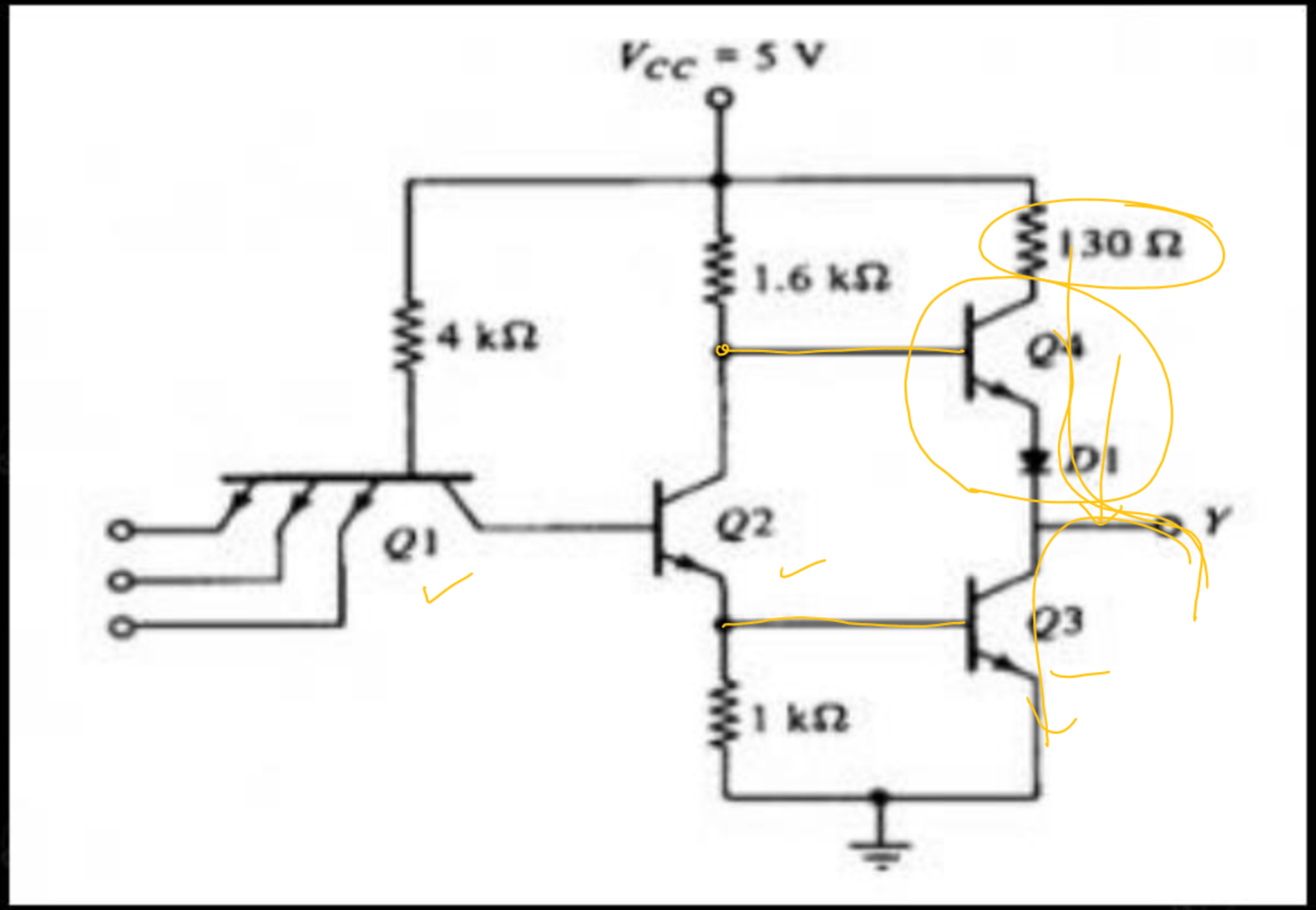
$V_o = 0$

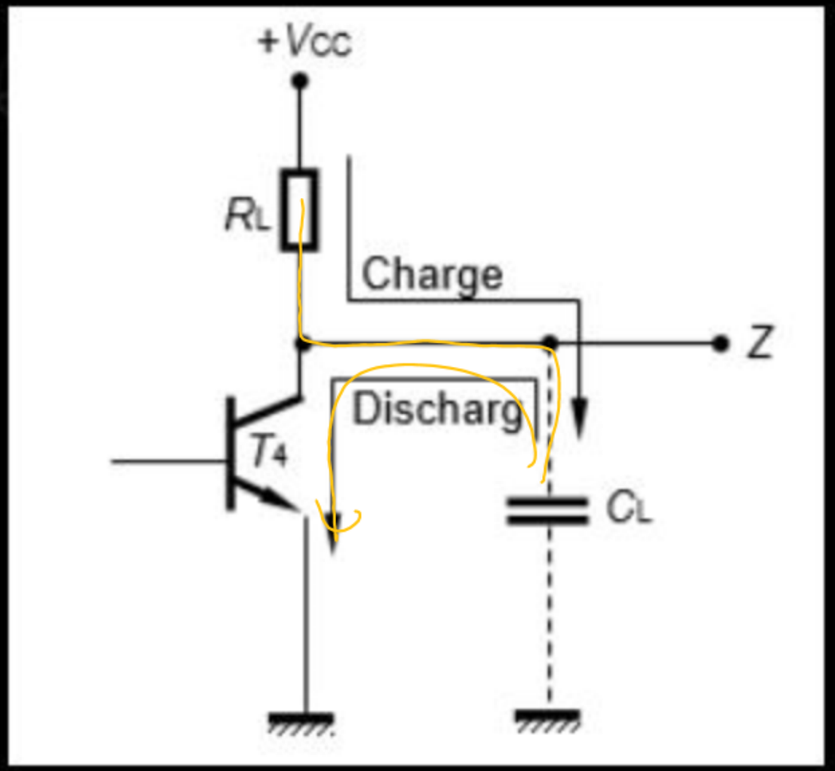
$R_{C3}$ = high

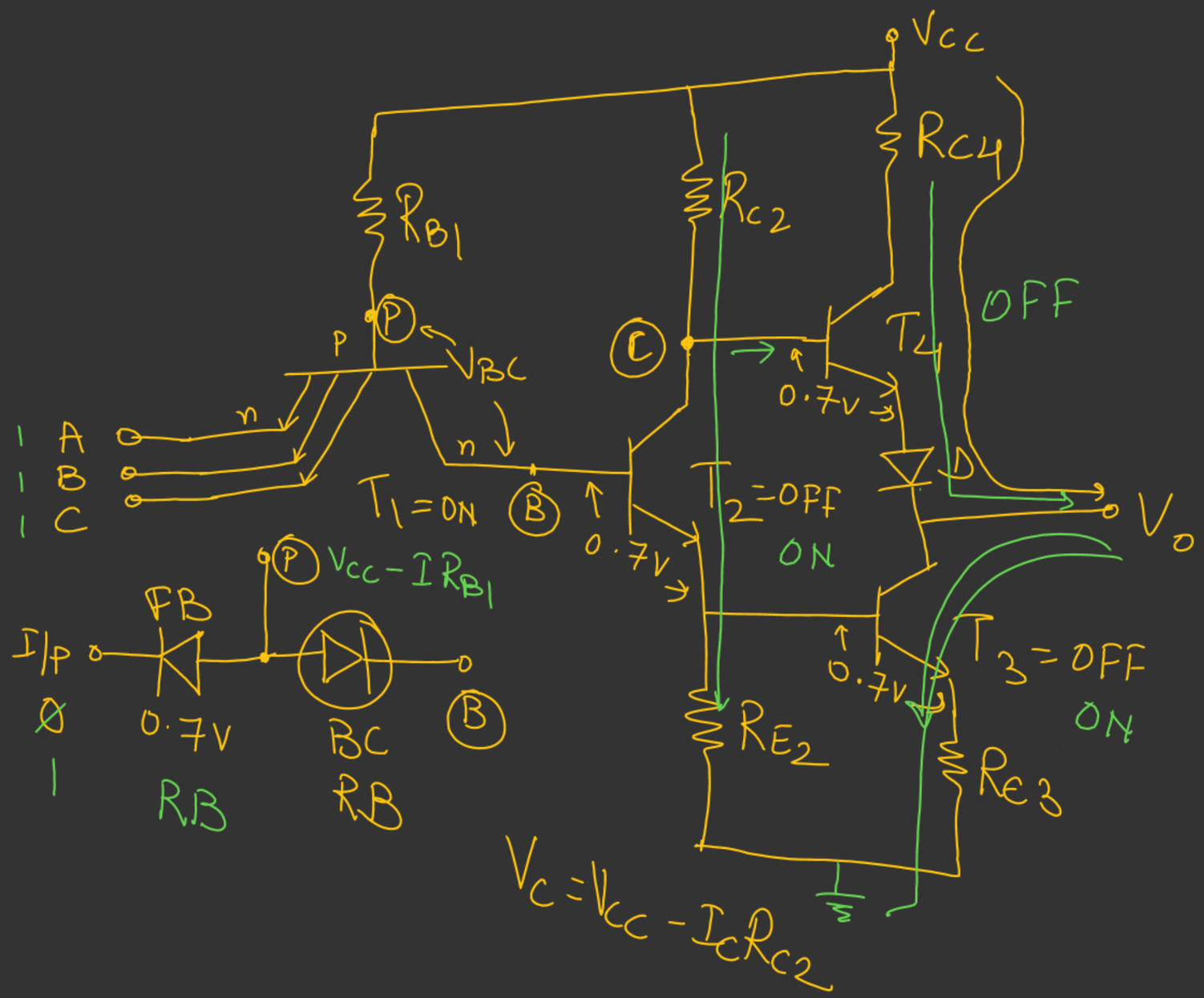
# Totem pole TTL

- Totem Pole means the addition of an active pull up circuit in the output of the gate
- This results in a reduction of propagation delay.
- Logic operation is the same as the open collector output.
- The use of transistors Q4 and diode is to provide quick charging and discharging of parasitic capacitance across Q3.
- The resistor is used to keep the output current to a safe value.
- Advantages: Fast switching times due to the push-pull arrangement of the transistors. Can drive both high and low loads.
- External pull up resistor is not required.
- Disadvantage: Output of two gates cannot be tied together.

# Totempole TTL NAND Gate

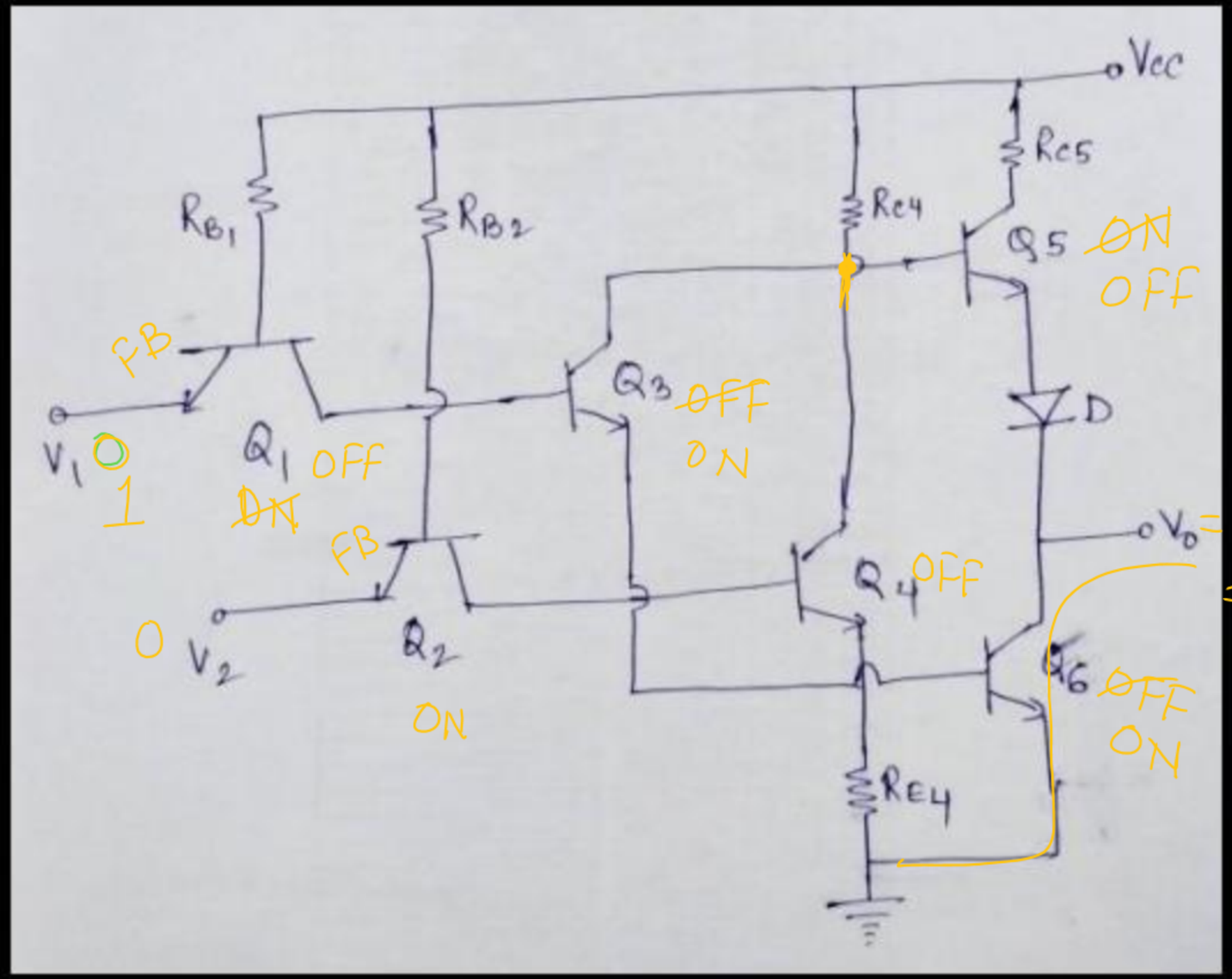





| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

# Totem pole TTL NOR Gate:

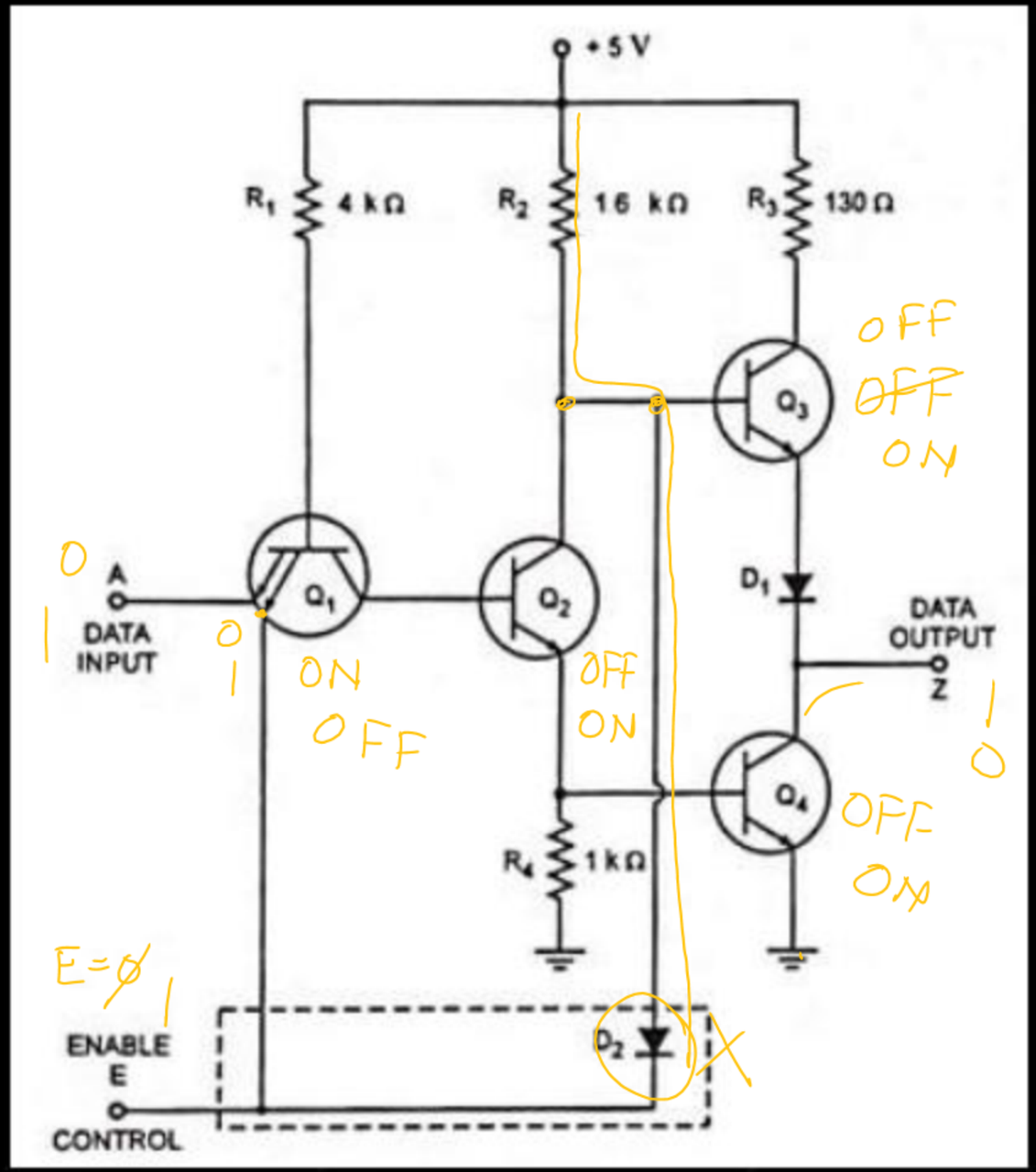



NOR

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 ✓ |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

# Three state Gate

- Totem-pole outputs cannot be connected together due to very large current drain from the supply and consequent heating of ICs which may get damaged.
- Open collector outputs can be connected together with a common collector resistor connected externally. This causes the problems of loading and operation speed.
- To overcome these difficulties, special circuits have been developed in which there is one more state of output, referred to as the third state or high impedance (Hi-Z) state, in addition to low and high states. Such circuits are called Tristate or three state logic.
- The tristate logic circuit utilizes the high speed operation of the totem-pole arrangement while permitting outputs to be wiredANDed (connected together).
- It provides 3 state output.
- Low-level state when a lower transistor is ON and an upper transistor is OFF.
- High-level state when the lower transistor is OFF and the upper transistor is ON.
- Third state when both transistors are OFF. It allows a direct wire connection of many outputs.



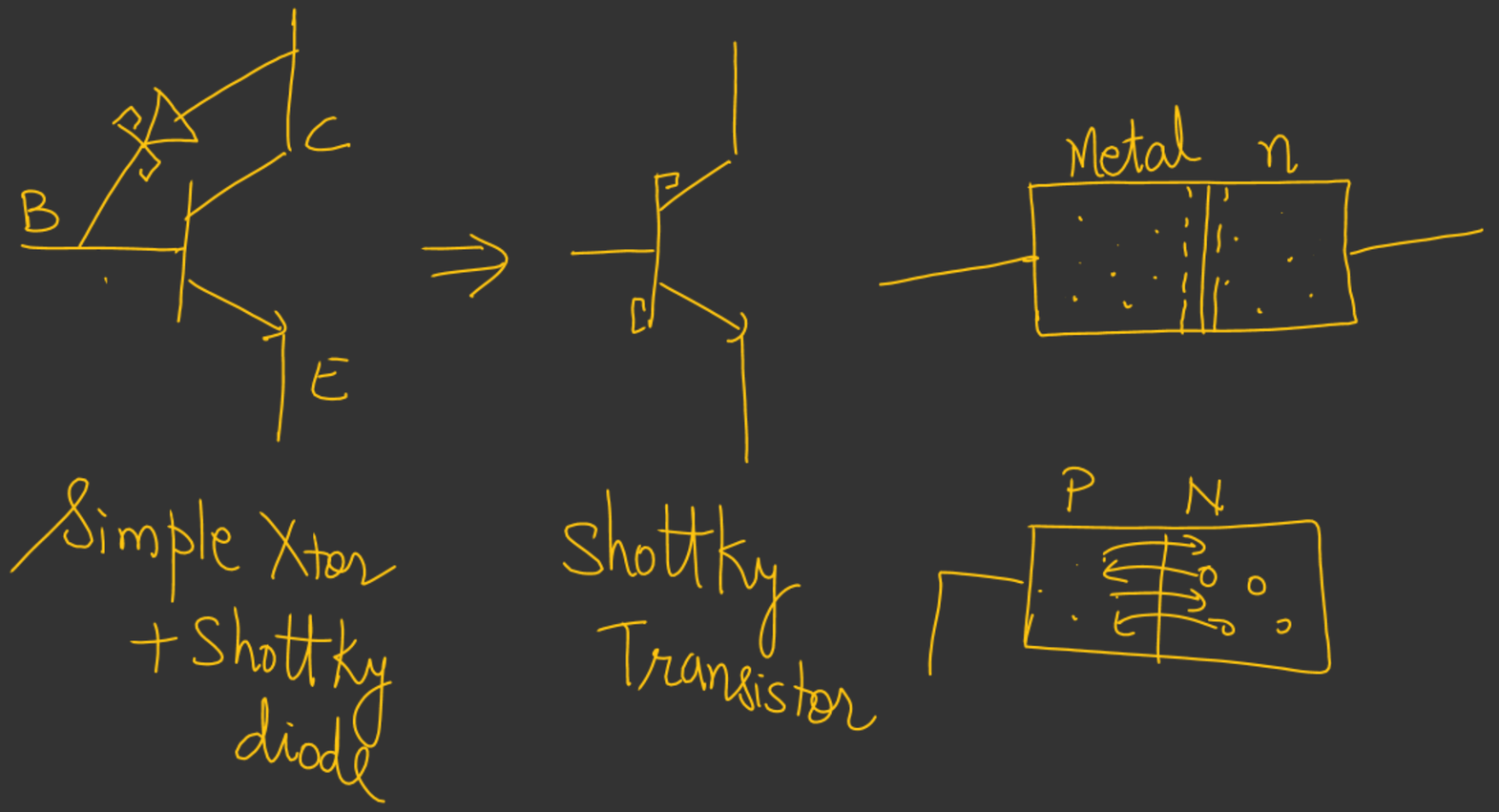

- When E = 0, the circuit goes into its Hi-Z state regardless of the state of logic input A.
- The low at E forward-biases the emitter-base junction of transistor Q1 and shunts the resistor R1 current away from transistor Q2 so that Q2 turns off, which turns transistor Q4 off.
- The low at E also forward biases diode D2 to shunt current away from the base of transistor Q3, so that Q3 also turns off.
- With both totem-pole transistors in the off-state, the output terminal is essentially an open circuit.

# Truth Table for TTL Inverter

| Data Input (A) | Control (E) | Data Output |
|---|---|---|
| 0 | 0 | High Z |
| 1 | 0 | High Z |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

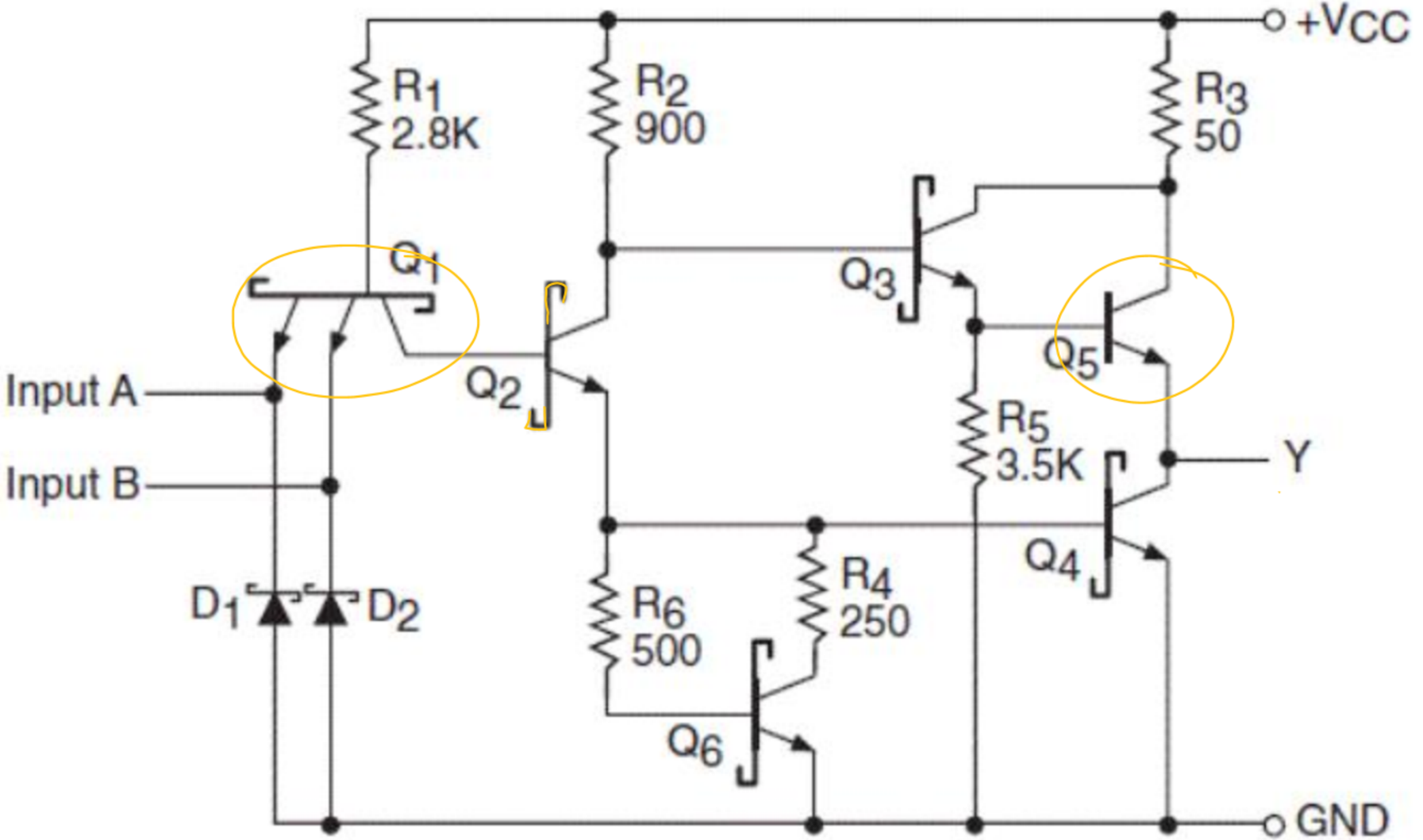
# Schottky TTL

- A relatively fast bipolar logic family
- Its internal configuration is similar to normal TTL except that Schottky transistors are used.
- Schottky transistors consist of a normal bipolar transistor with a Schottky diode connected across the base-collector junction.
- The Schottky diode is a semiconductor-metal diode that has a low cut-in voltage (forward bias voltage drop), typically 300 millivolts.
- It has a relatively high switching speed.
- In Schottky TTL the low cut-in voltage of the diode limits the base-collector voltage to about 400 mV, which prevents the transistor falling into saturation.
- This results in faster switching times for the transistors constructed in this way.




Simple Xtor + Shottky diode

Shottky Transistor


+Vcc
R1
2.8K
R2
900
R3
50
Q1
Q2
Q3
Q5
Input A
Input B
R5
3.5K
Y
Q4
D1
D2
R6
500
R4
250
Q6
GND

# UNIVERSITY QUESTIONS

| YEAR | QUESTIONS | MARKS |
|---|---|---|
| 22-23 | Draw and Explain a NAND gate in Totem Pole TTL Configuration. | 10 Marks |

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# Thank You