AKTU

GATEWAY CLASSES

Digital System Design

B.Tech. 3rd Sem

EC & Allied



Exam/Result Oriented Content

- ✓ Recorded Video Lectures
- ✓ Pdf Notes
- ✓ PYQs

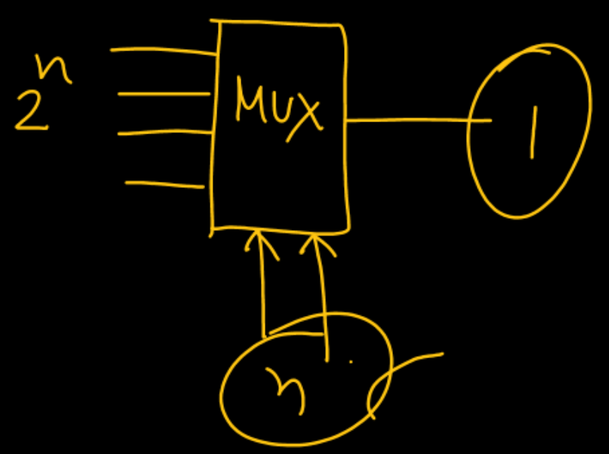
UNIT 2 : Combinational circuits

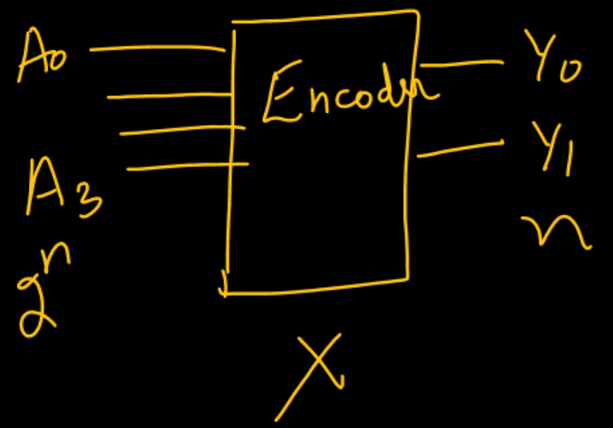
Today's Target

- Digital Encoder
- 4×2, 8×3, Priority Encoders
- University Questions

UNIVERSITY QUESTIONS

YEAR	QUESTION	MARKS
22-23	What is the difference between Multiplexer and Encoder	2 marks
18-19	Write short notes on priority encoder.	7 marks



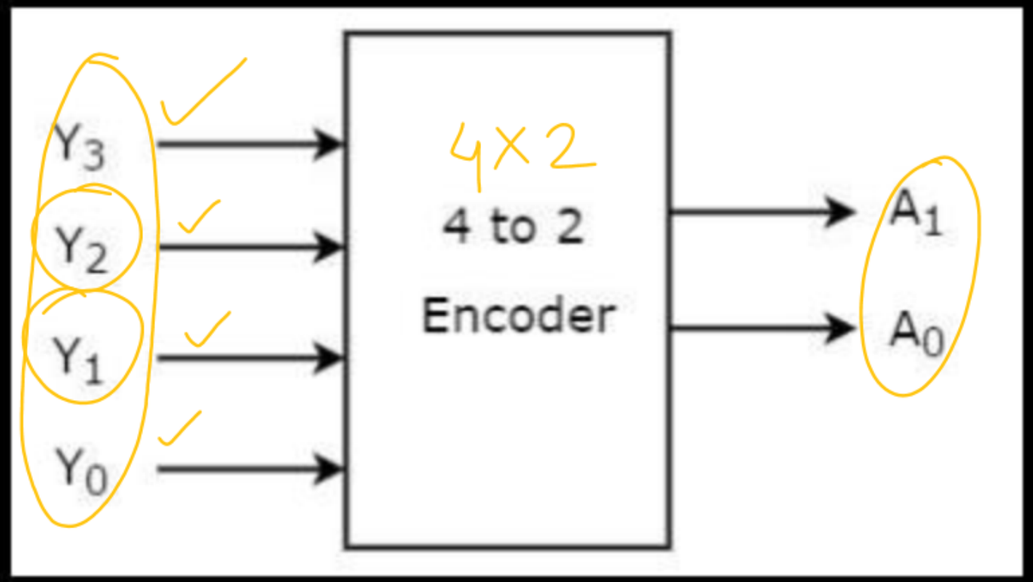


Digital Encoder

- a combinational circuit that generates a specific code at its outputs such as binary or BCD in response to one or more active inputs.
- reverse operation of Decoder
- 2^n input lines
- enable signal is optional in encoders

4 to 2 Encoder

- four inputs Y_3, Y_2, Y_1 & Y_0
- two outputs A_1 & A_0
- **block diagram** is shown
- At any time, only one of these 4 inputs can be '1' in order to get the respective binary code at the output.



Truth table

INPUTS				OUTPUTS	
Y3	Y2	Y1	Y0	A1	A0
1	0	0	0	1	1
0	1	0	0	1	0
0	0	1	0	0	1
0	0	0	1	0	0

Boolean Equations

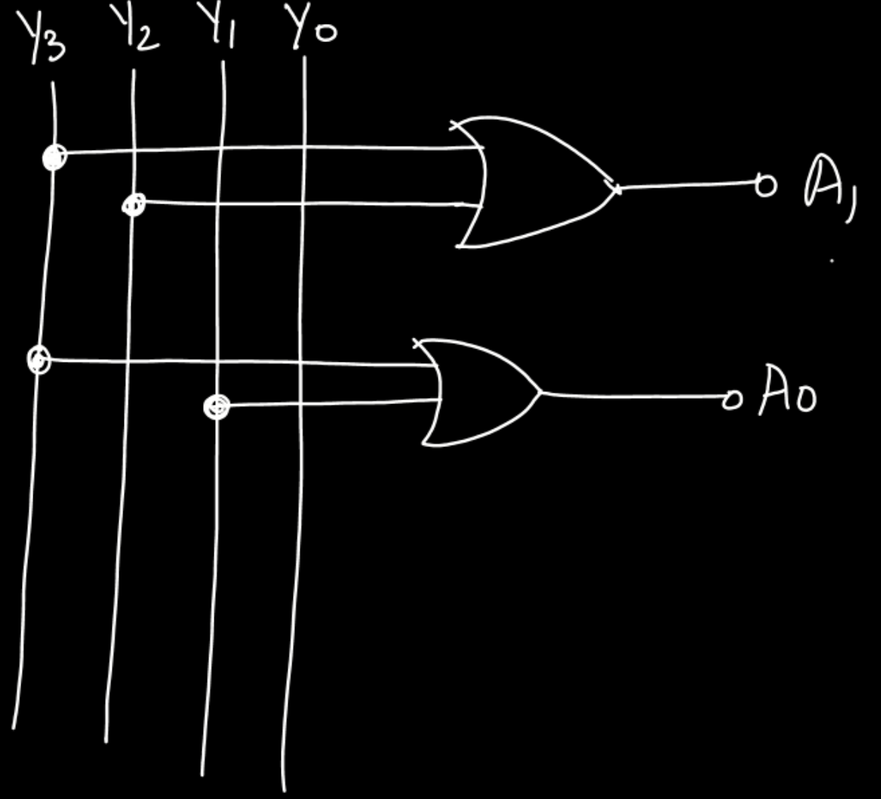
$A_1 = Y_3 + Y_2$

$A_0 = Y_3 + Y_1$

Implementation of 4 to 2 Encoder

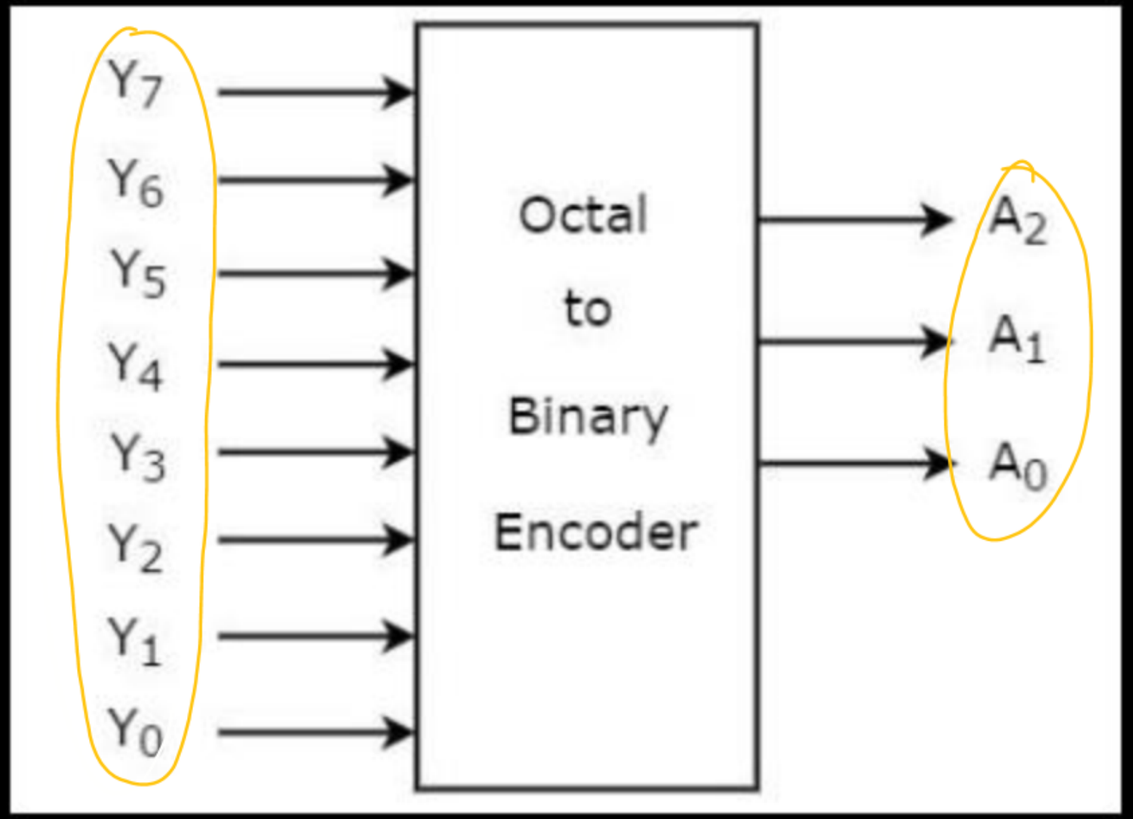
$$A_1 = Y_3 + Y_2$$

$$A_0 = Y_3 + Y_1$$



Octal to Binary Encoder

- eight inputs, Y_7 to Y_0
- three outputs A_2, A_1 & A_0
- **block diagram** of octal to binary Encoder



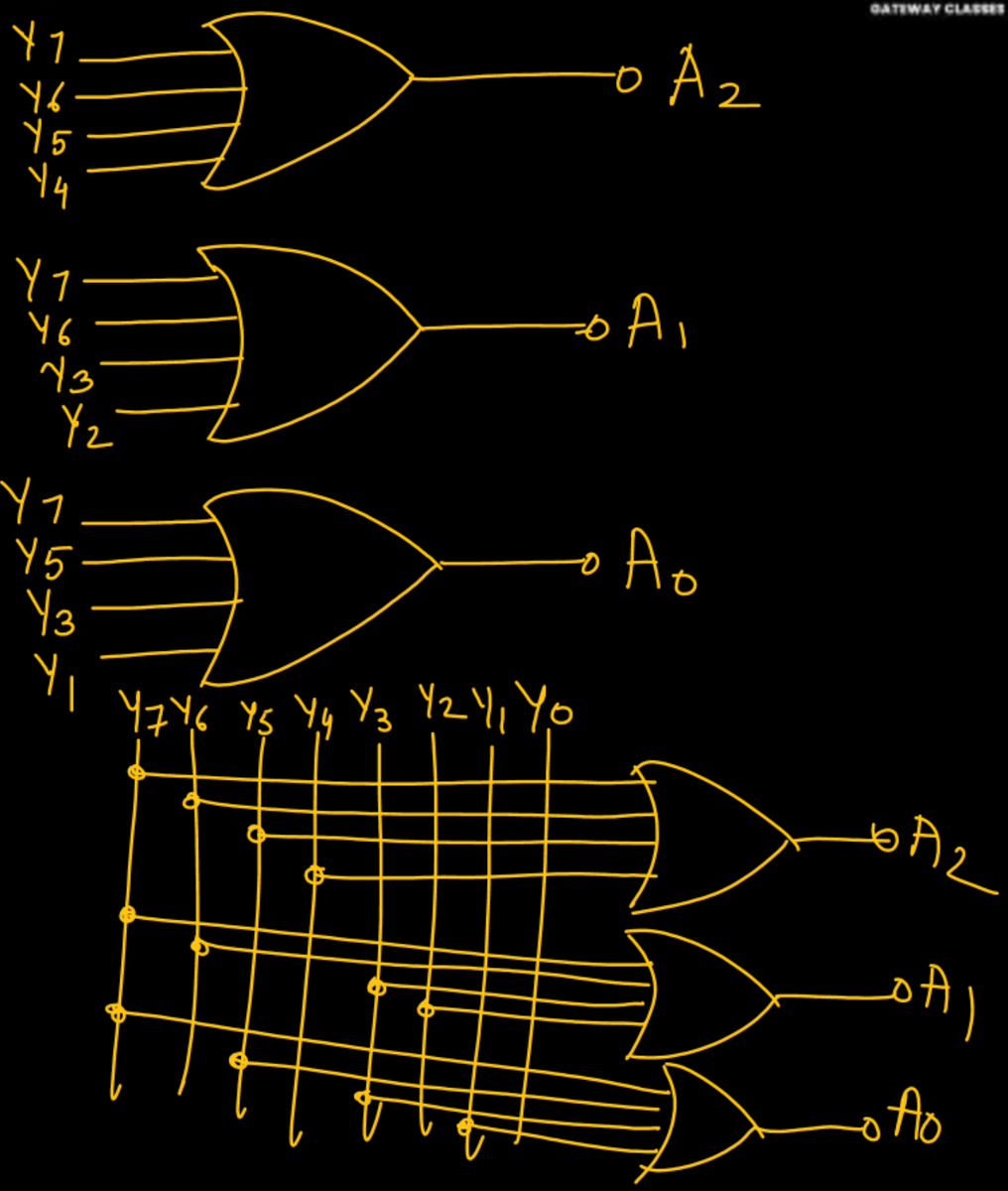
Truth table & Boolean Equations

INPUTS								OUTPUTS		
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	A2	A1	A0
1	0	0	0	0	0	0	0	1	1	1
0	1	0	0	0	0	0	0	1	1	0
0	0	1	0	0	0	0	0	1	0	1
0	0	0	1	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0

$A_2 = Y_7 + Y_6 + Y_5 + Y_4$

$A_1 = Y_7 + Y_6 + Y_3 + Y_2$

$A_0 = Y_7 + Y_5 + Y_3 + Y_1$



Priority Encoder

- 4 to 2 priority encoder
- four inputs Y_3, Y_2, Y_1 & Y_0
- two outputs A_1 & A_0
- Y_3 has the highest priority
- Y_0 has the lowest priority
- if more than one input is '1' at the same time, the output will be the binary code corresponding to the input, which is having **higher priority**.
- one more **output, V** ensures the code available at outputs is valid or not.
- If at least one input of the encoder is '1', then V=1
- If all the inputs of encoder are '0', then V=0

Truth table of 4 to 2 priority encoder

INPUTS				OUTPUTS		
Y3	Y2	Y1	Y0	A1	A0	V
0	0	0	0			
0	0	0	1			

K-maps for A1 & A0

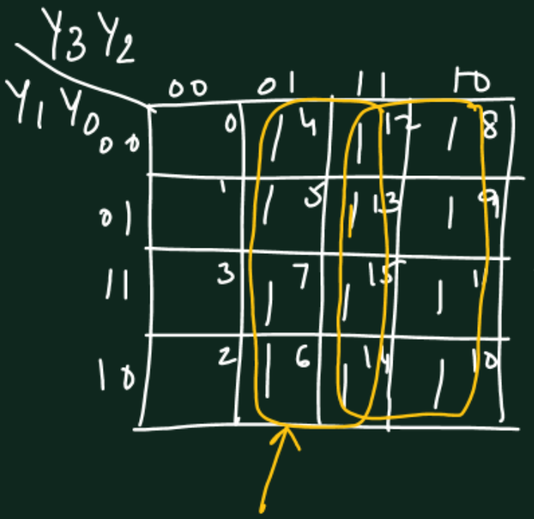
$A_1 = Y_2 + Y_3$

$A_0 = Y_3 + \overline{Y}_2 Y_1$

$V = Y_3 + Y_2 + Y_1 + Y_0$

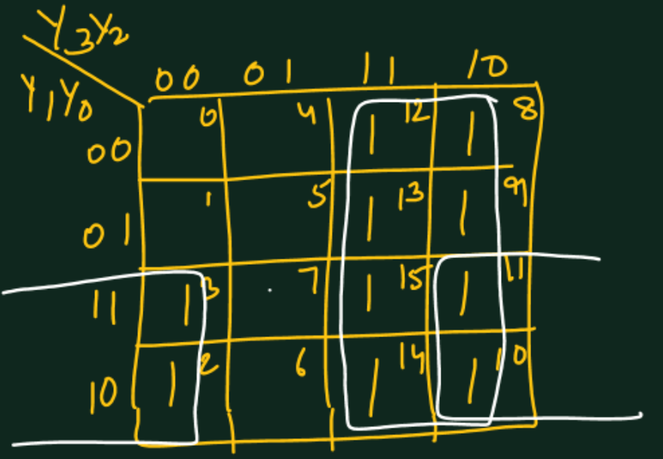
I/P						
Y_3	Y_2	Y_1	Y_0	A_1	A_0	V
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	1	1
0	1	0	0	0	1	1
0	1	0	1	0	1	1
0	1	1	0	0	1	1
0	1	1	1	0	1	1
1	0	0	0	0	1	1
1	0	0	1	0	1	1
1	0	1	0	0	0	1
1	0	1	1	0	0	1
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	0	1

for A_1



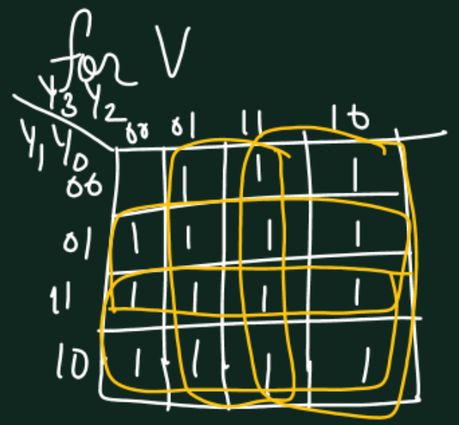
$A_1 = Y_2 + Y_3$

for A_0



$A_0 = Y_3 + \overline{Y_2} Y_1$

for V



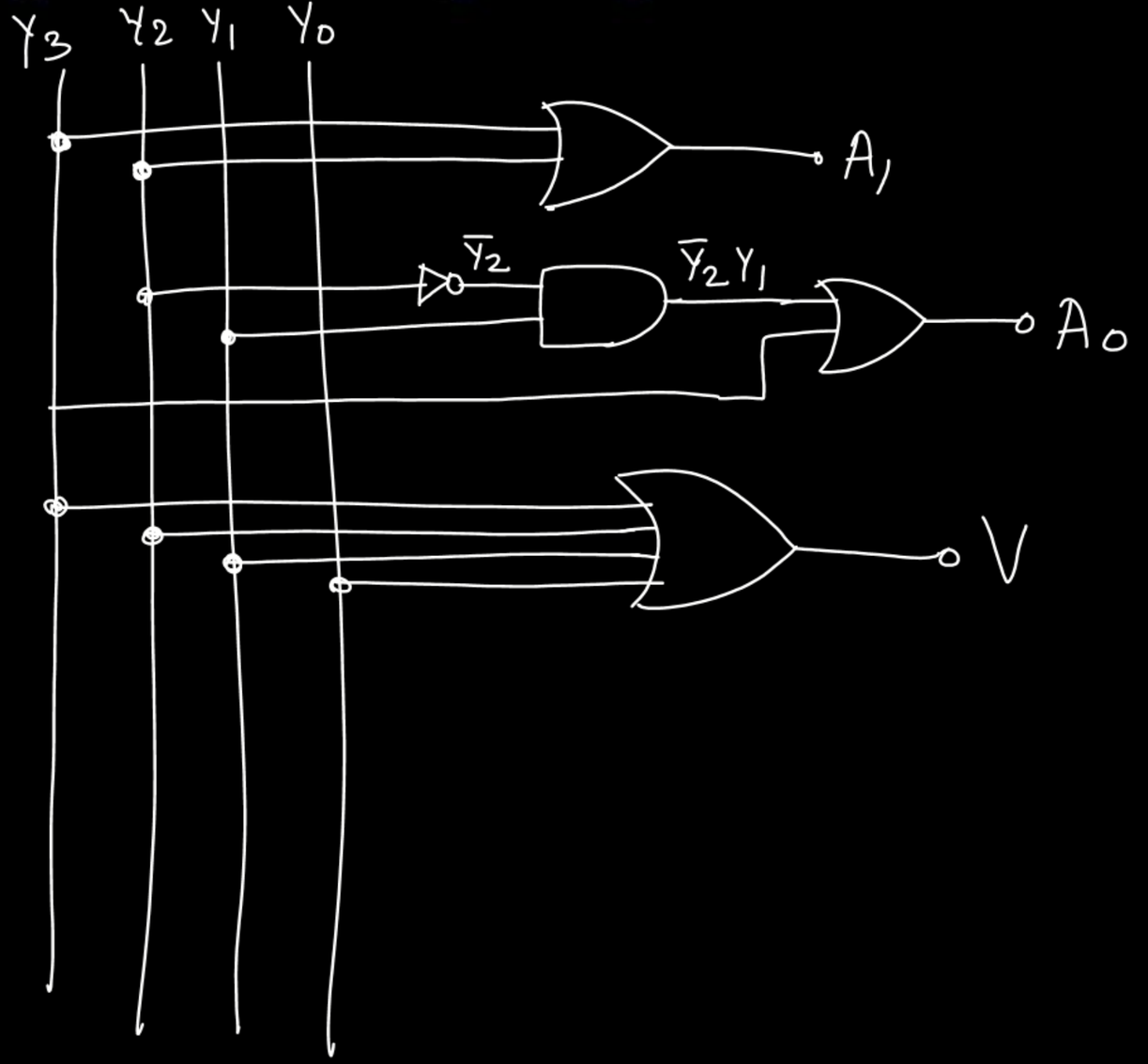
$V = Y_3 + Y_2 + Y_1 + Y_0$

Circuit Diagram of 4 to 2 priority encoder

$A_1 = Y_3 + Y_2$

$A_0 = Y_3 + \bar{Y}_2 Y_1$

$V = Y_3 + Y_2 + Y_1 + Y_0$



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Link in Description

Thank You

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