AKTU

GATEWAY CLASSES

Digital System Design

B.Tech. 3rd Sem

EC & Allied



Exam/Result Oriented Content

- ✓ Recorded Video Lectures
- ✓ Pdf Notes
- ✓ PYQs

DIGITAL SYSTEM DESIGN

UNIT 3 : Sequential logic design

Lec 7

Today's Target

- Digital Registers
- Serial Input Serial Output
- Serial Input Parallel Output
- Parallel Input Parallel Output
- Parallel Input Serial Output

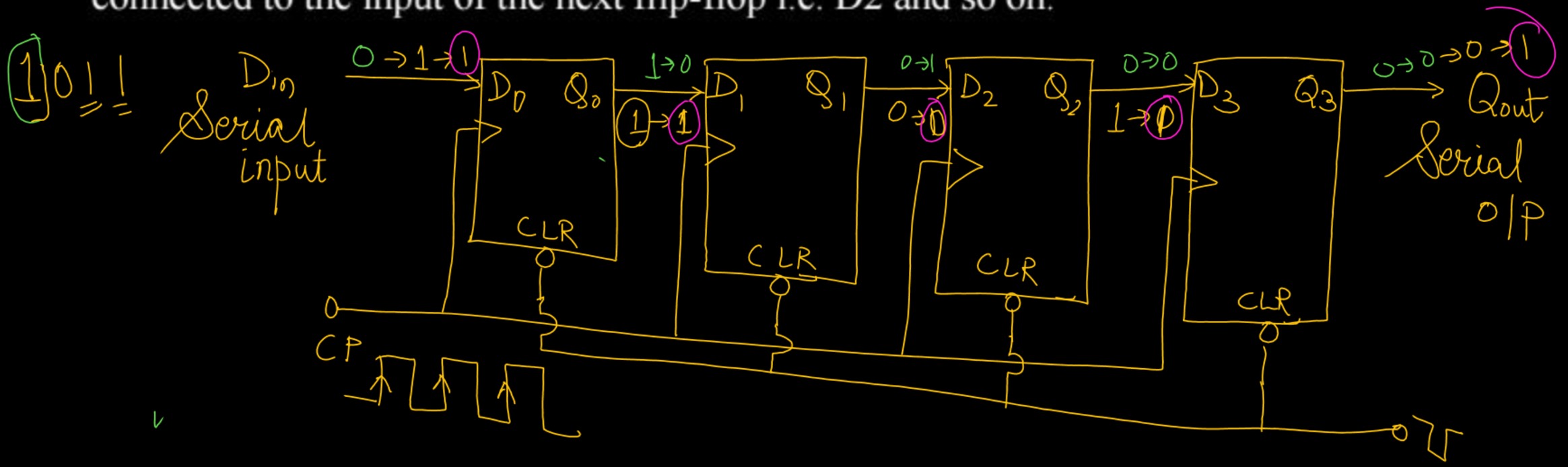
Digital Registers

- One flip-flop can store one-bit of information.
- In order to store multiple bits of information, we require multiple flip-flops.
- The group of flip-flops, which are used to hold store the binary data is known as **register**.
- If the register is capable of shifting bits either towards right hand side or towards left hand side is known as shift register.
- An 'N' bit shift register contains 'N' flip-flops.
- Following are the four types of shift registers based on applying inputs and accessing of outputs.
- Serial Input Serial Output — SISO
- Serial Input Parallel Output — SIPO
- Parallel Input Serial Output — PISO
- Parallel Input Parallel Output — PIPO

Serial Input Serial Output

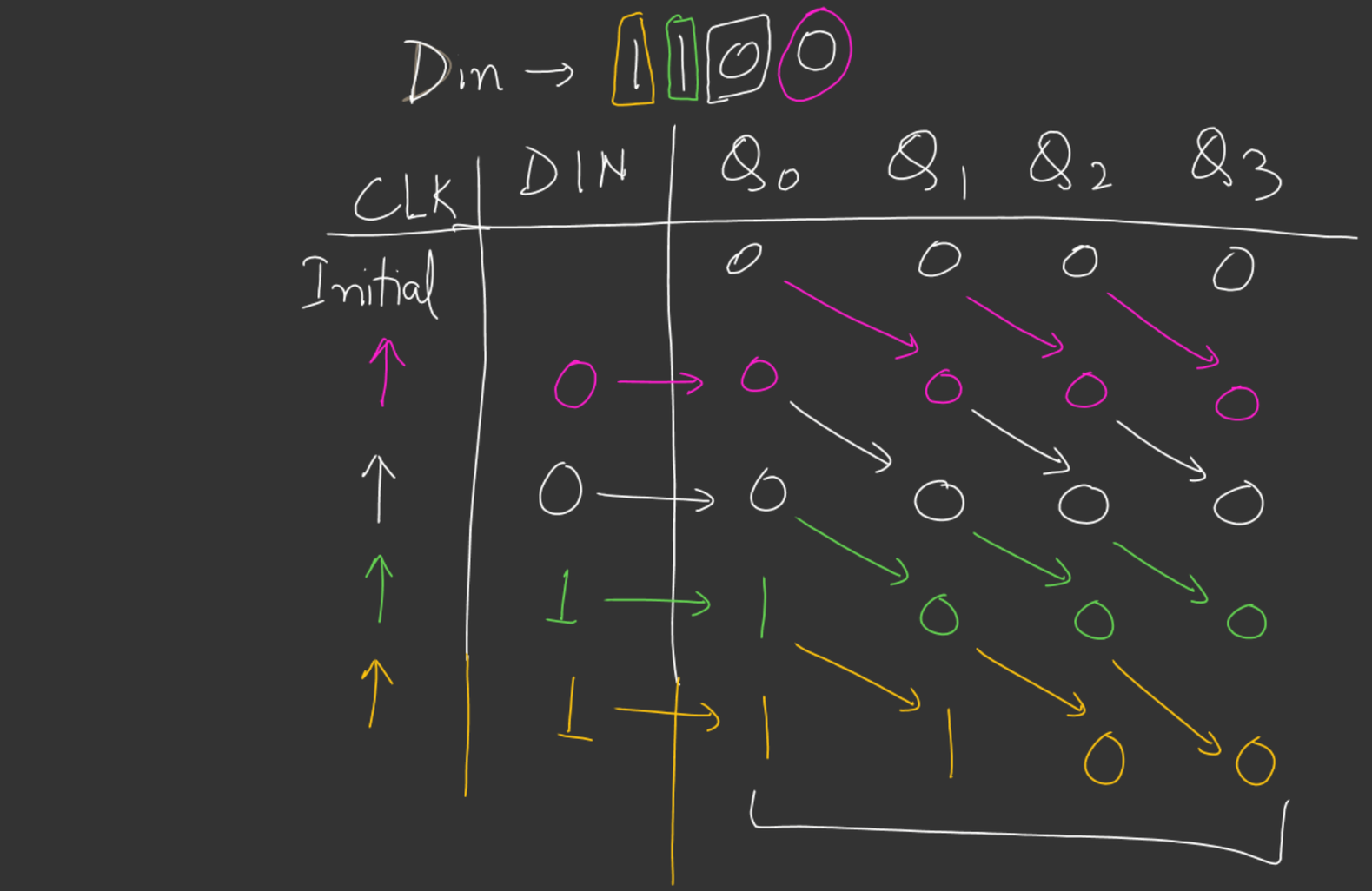
SISO

- Let all the flip-flop be initially in the reset condition i.e. Q3 = Q2 = Q1 = Q0 = 0.
- If an entry of a four bit binary number 1 1 1 1 is made into the register, this number should be applied to Din bit with the LSB bit applied first.
- The D input of FF-3 i.e. D3 is connected to serial data input Din. Output of FF-3 i.e. Q3 is connected to the input of the next flip-flop i.e. D2 and so on.



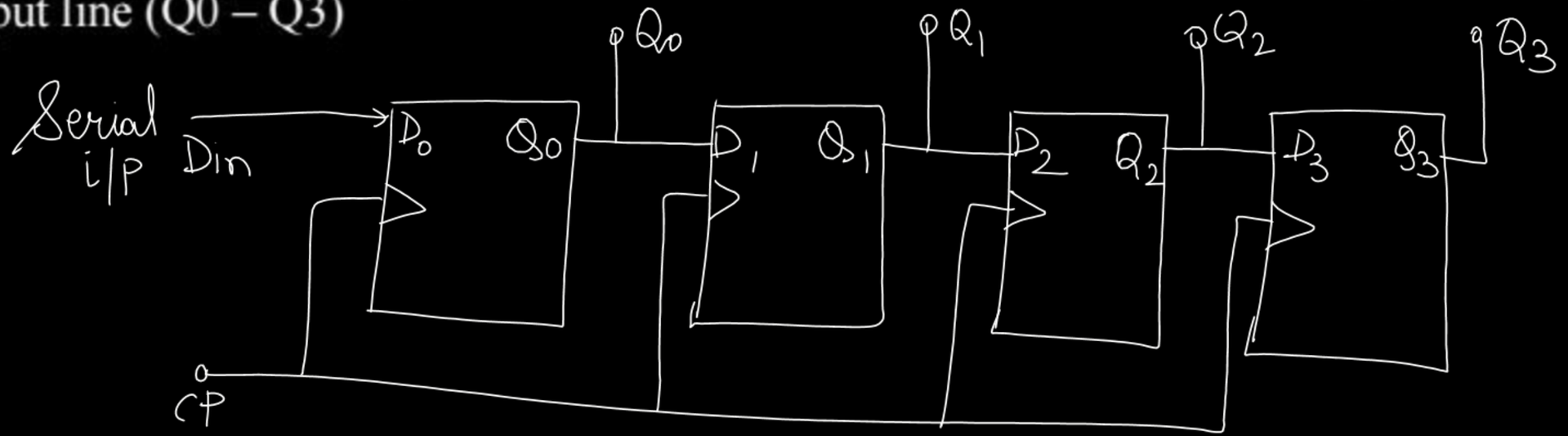
Truth Table

CLK	Din	Q3	Q2	Q1	Q0
Initially	1 0 1 1	0	0	0	0
↑	1	1	0	0	0
↑	0	0	1	0	0
↑	1	1	0	1	0
↑	1	1	1	0	1


Din → 1100
CLK
DIN
Q0
Q1
Q2
Q3
Initial

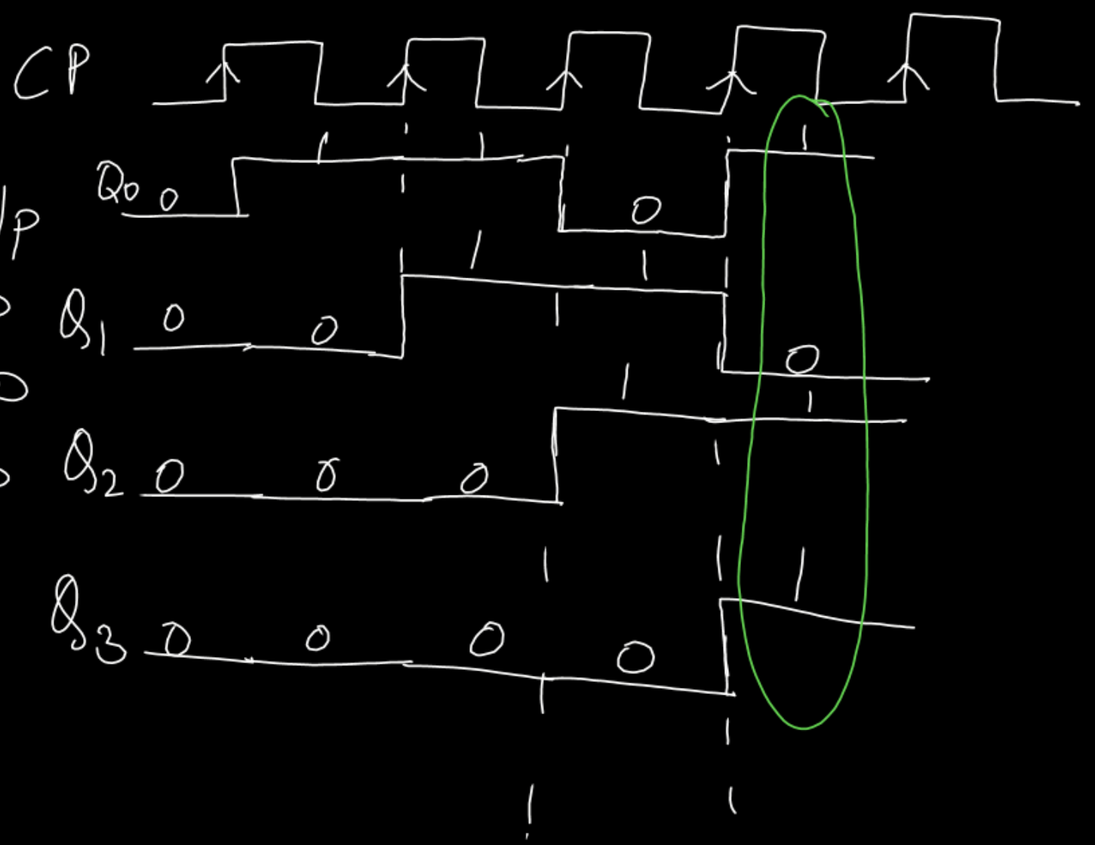
Serial in – Parallel out Shift Register

- used for the conversion of data from serial to parallel.
- The data comes in one after the other per clock cycle and can either be shifted and replaced or be read off at each output.
- This means when the data is read in, each read in bit becomes available simultaneously on their respective output line (Q0 – Q3)



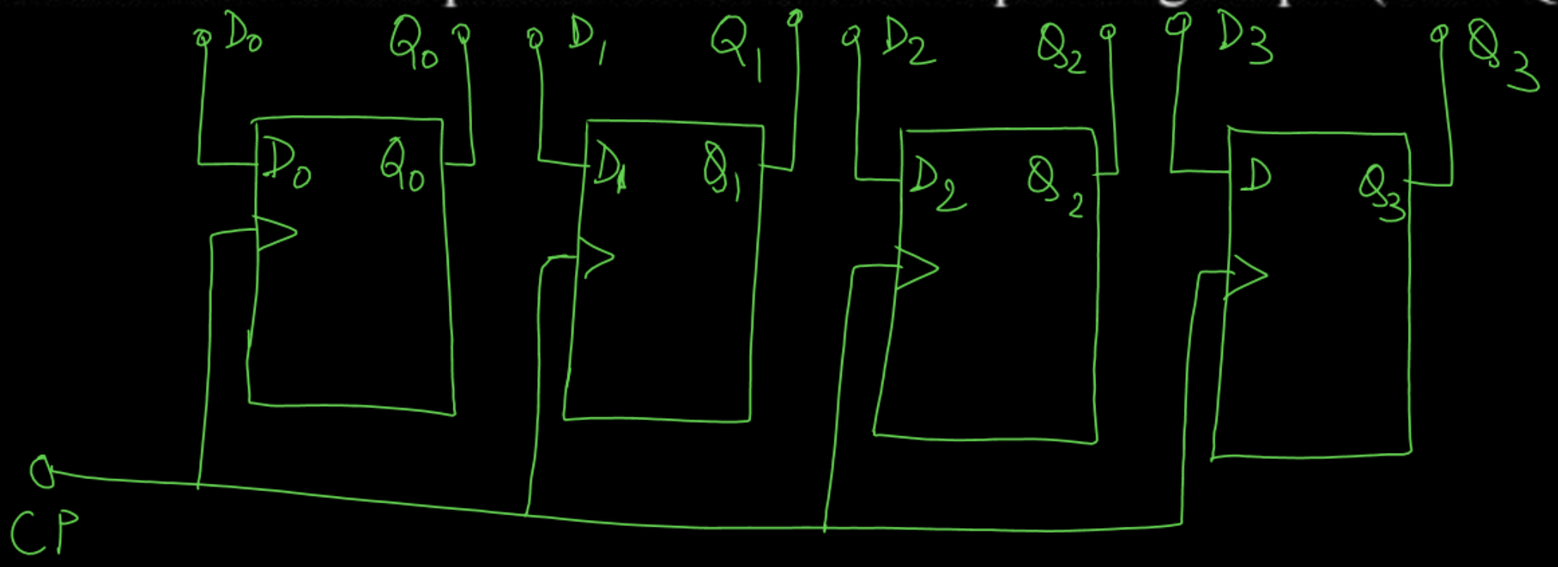
Truth Table & Waveforms

	FF0	FF1	FF2	FF3	
CLEAR	0	0	0	0	← CLK 1 O/P
1011	1	0	0	0	← CLK 2 O/P
	1	1	0	0	← CLK 3 O/P
	0	1	1	0	← CLK 4 O/P
	1	0	1	1	



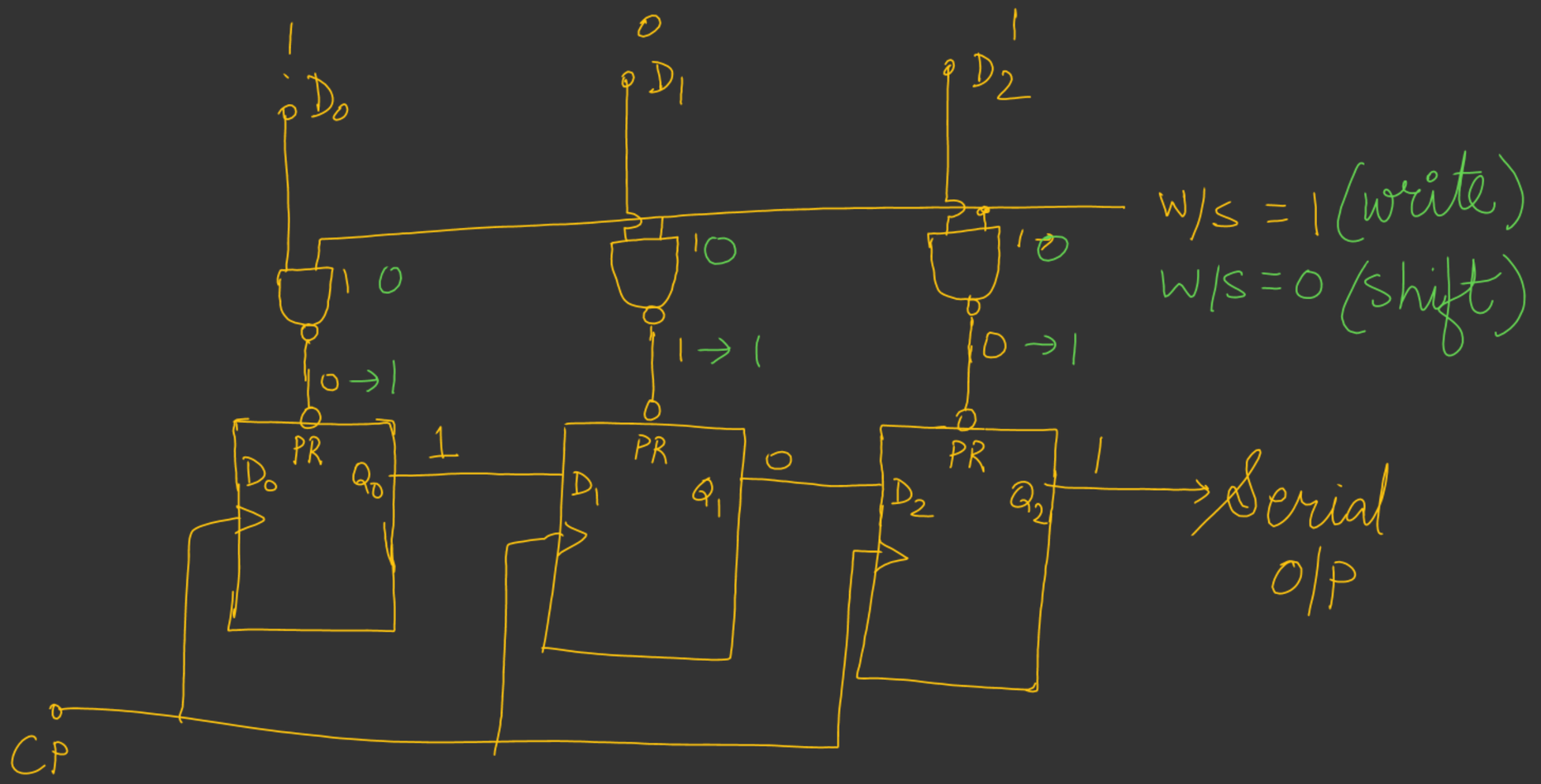
Parallel in – Parallel out shift register

- The output data across the parallel outputs appear simultaneously as the input data is fed in.
- The input data at each of the input pins from D0 to D3 are read in at the same time when the device is clocked and at the same time and passed out at the corresponding output (from Q0 to Q3).



Parallel in – Serial out Shift Register

- The data is supplied in parallel.
- This register can be used to store and shift a 4-bit word, with the write/shift (W/S) control input controlling the mode of operation of the shift register.
- When the W/S =1 (Write Mode), data can be written and clocked in via D0 to D3.
- When W/S =0 (Shift mode), the register then shifts the data out serially on clock input.


1
D0
0
D1
1
D2
W/S = 1 (write)
W/S = 0 (shift)
1 0
1 0
1 0
0 → 1
1 → 1
0 → 1
PR
D0
Q0
1
PR
D1
Q1
0
PR
D2
Q2
1
Serial O/P
CP

GATEWAY CLASSES

AKTU Full Courses (Paid)

Download Gateway Classes Application

From Google Play store

All Subjects

Link in Description

Thank You