AKTU

GATEWAY CLASSES

Digital System Design

B.Tech. 3rd Sem

EC & Allied



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DIGITAL SYSTEM DESIGN

UNIT 3 : Sequential logic design

Lec 8

Today's Target

- Finite State Machines
- Mealy State Machine
- Moore State Machine
- Numerical
- University Questions

Finite State Machines

- We know that synchronous sequential circuits change or affect their states for every positive or negative transition of the clock signal based on the input.
- This behavior of synchronous sequential circuits can be represented in the graphical form and it is known as state diagram.

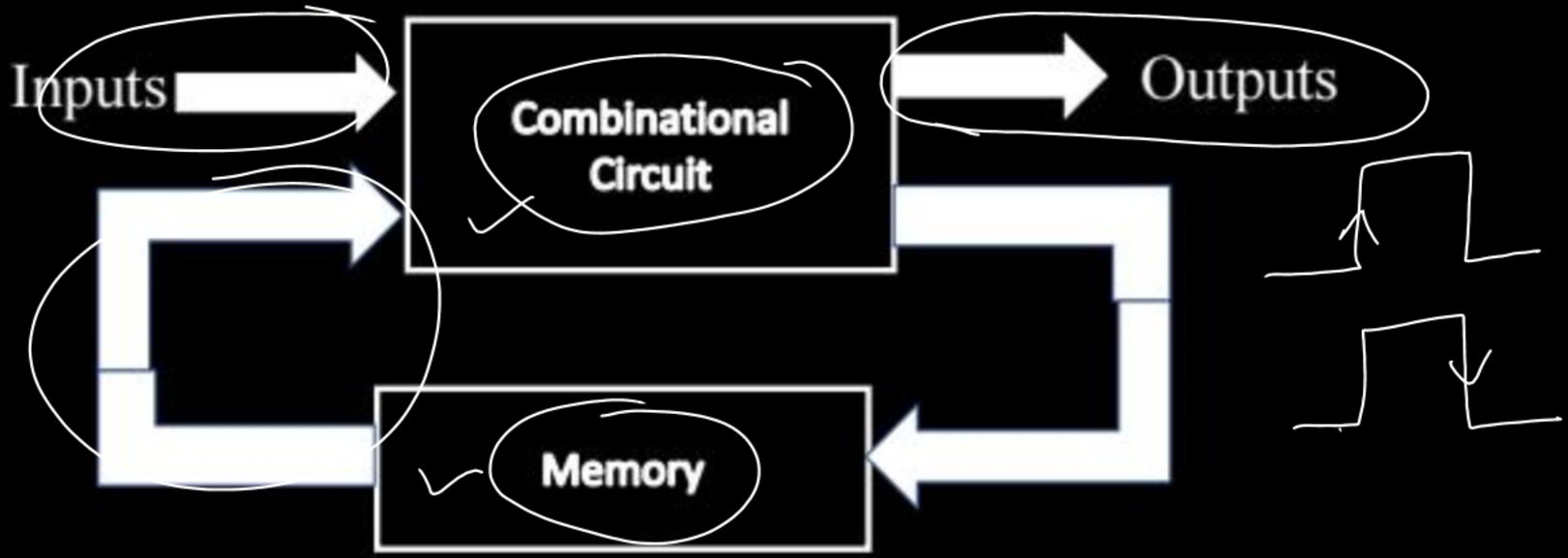


- A synchronous sequential circuit is also called as Finite State Machine FSM, if it has finite number of states.
- There are two types of FSMs.

  1) Mealy State Machine
  2) Moore State Machine

Mealy State Machine

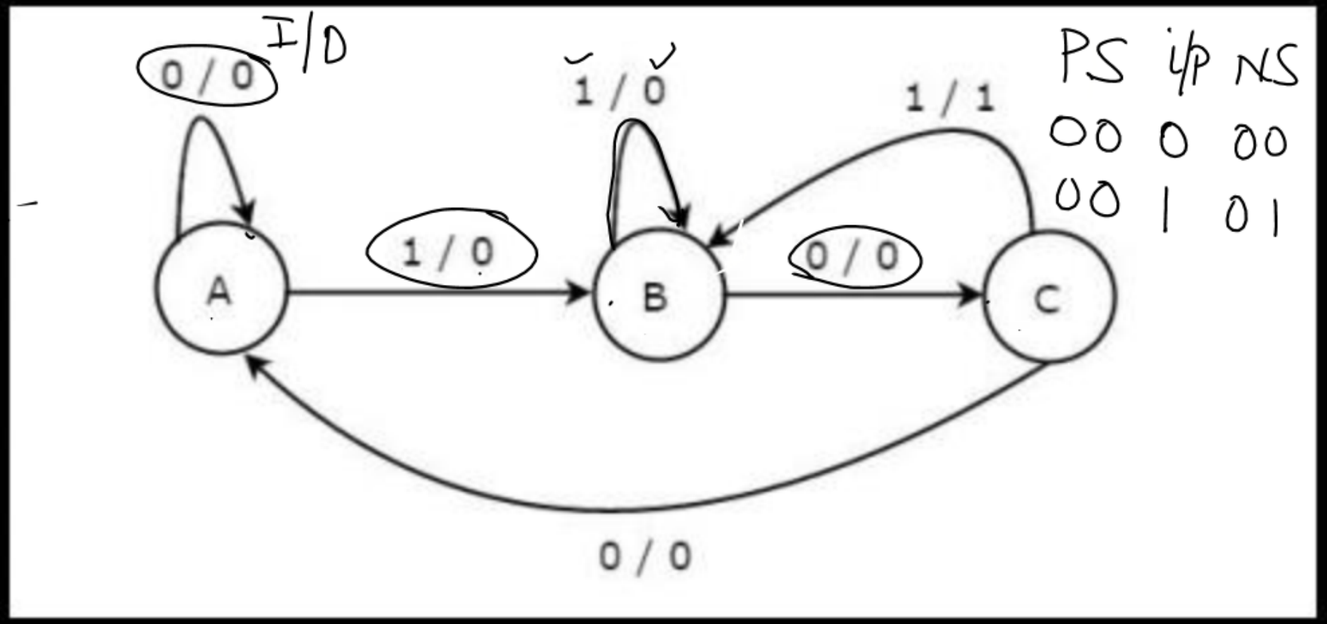
- A Finite State Machine is said to be Mealy state machine, if outputs depend on both present inputs & present states.
- The block diagram of Mealy state machine is shown in the following figure:

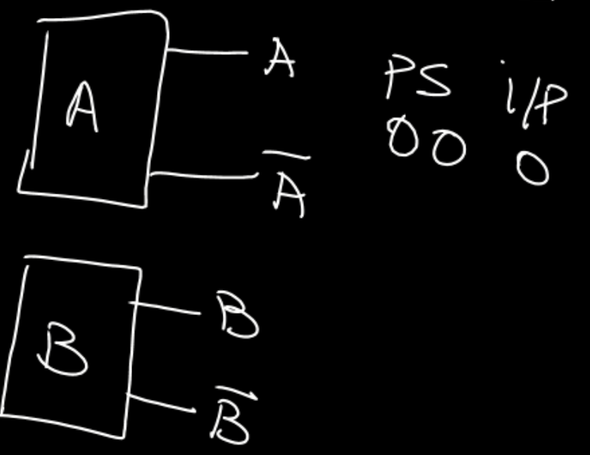


- two parts present in Mealy state machine: combinational logic and memory
- the outputs will be valid only at positive or negative transition of the clock signal.

State Diagram of Mealy state machine

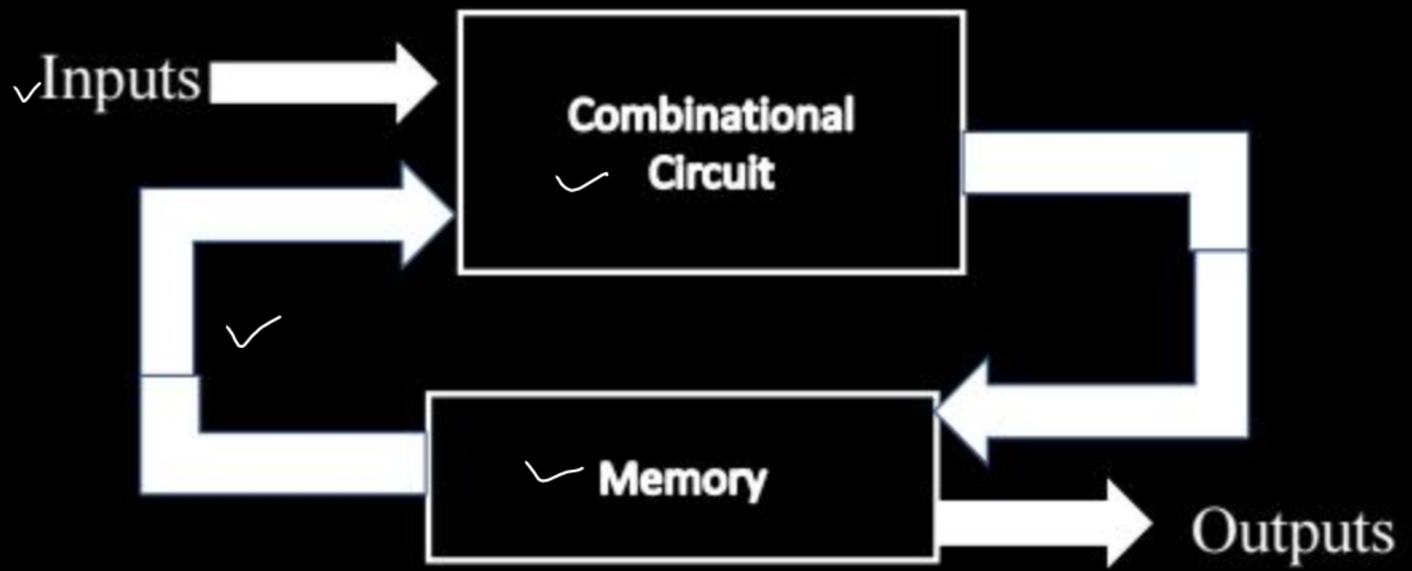
- Suppose, there are three states, namely A, B & C.
- These states are labelled inside the circles & each circle corresponds to one state.
- Transitions between these states are represented with directed lines.
- Here, 0 / 0, 1 / 0 & 1 / 1 denotes input / output.
- In the figure, there are two transitions from each state based on the value of input (x).
- In general, the number of states required in Mealy state machine is less than or equal to the number of states required in Moore state machine.





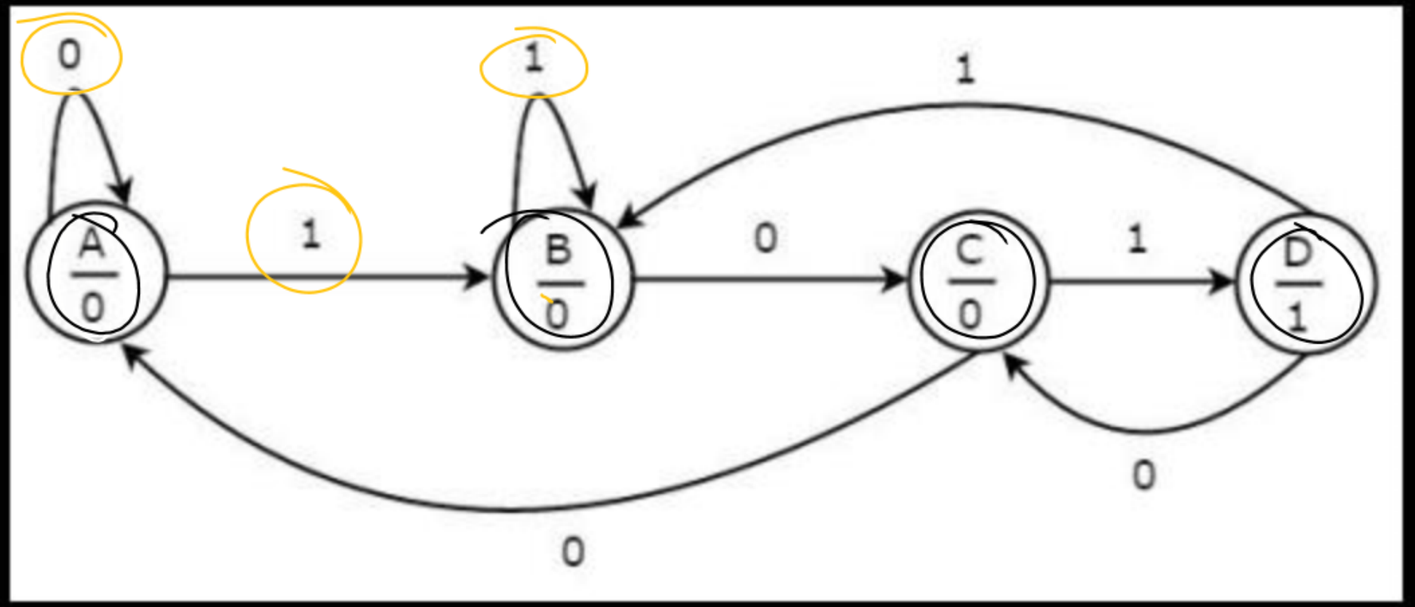
Moore State Machine

- A Finite State Machine is said to be Moore state machine, if outputs depend only on present states.
- two parts present in Moore state machine: combinational logic and memory.
- the present inputs and present states determine the next states.
- the outputs will be valid only after transition of the state.
- The block diagram of Moore state machine is shown in the following figure.

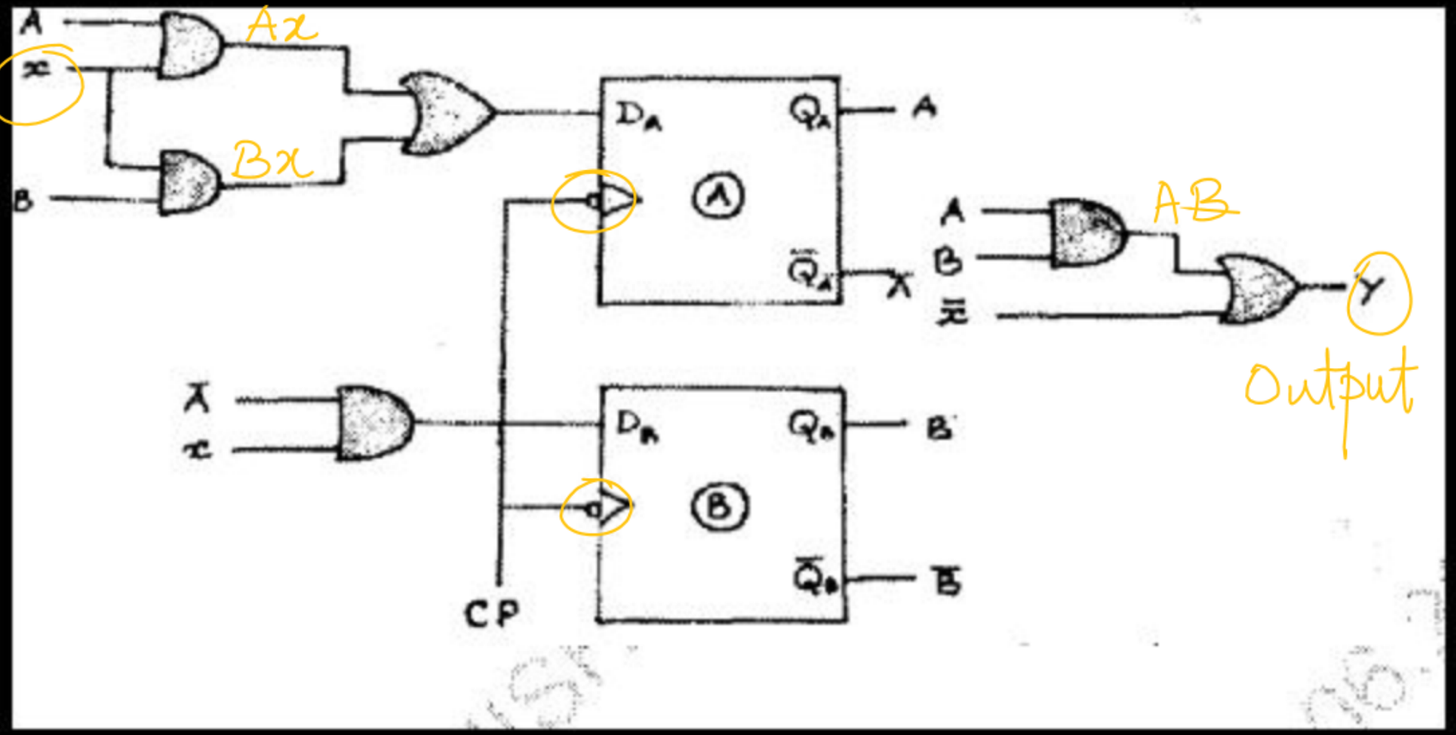


State Diagram of Moore state machine

- Suppose, there are four states, namely A, B, C & D.
- These states and the respective outputs are labelled inside the circles.
- Here, only the input value is labeled on each transition.
- In the figure, there are two transitions from each state based on the value of input, x.
- In general, the number of states required in Moore state machine is more than or equal to the number of states required in Mealy state machine.



Derive the state table and state diagram for the Sequential circuit shown in fig, (18-19)



Input

State Equations

$D_A = Ax + B\bar{x} = A$

$D_B = \bar{A}x = B$

$Y = AB + \bar{x}$

$$A_{n+1} = Ax + Bx$$

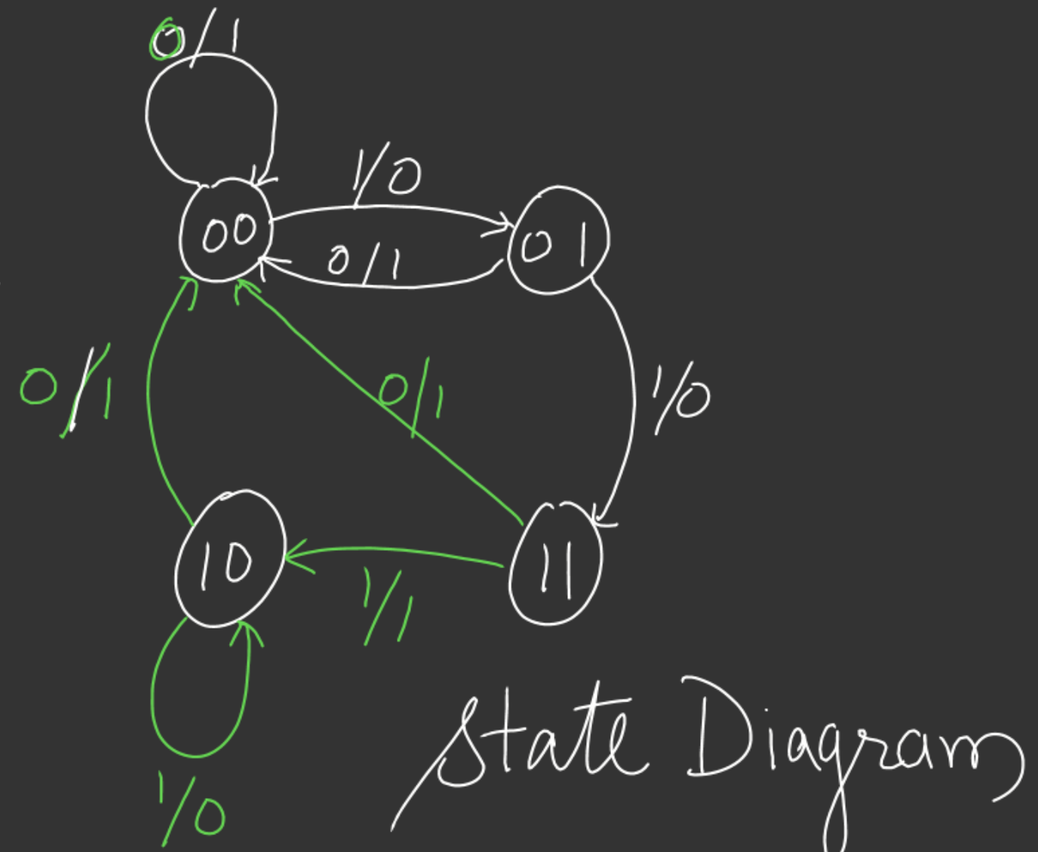
$$B_{n+1} = \bar{A}x$$

$$y = AB + \bar{x}$$

State Table

Present state		Input	Next State		output
A	B	x	A_{n+1}	B_{n+1}	Y
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	1

A	B	X	A_{n+1}	B_{n+1}	Y
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	1



State Diagram

University Questions

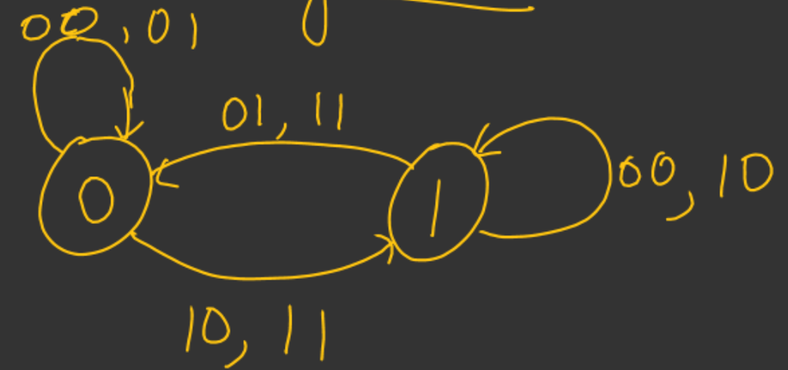
Year	Questions	Marks
21-22	Draw and explain block diagram of Moore model and Mealy model.	5 Marks
20-21	For the clocked JK flip-flop write the state table, draw the state diagram and the state equation.	10 Marks
20-21, 19-20	Discuss Mealy and Moore FSM. What do you mean by excitation table?	10 Marks

Clocked JK-FF

J	K	Q	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

State Table

State Diagram



For Q_{n+1}

Q_n \ JK	00	01	11	10
0			1	1
1	1			1

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

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Thank You