AKTU

GATEWAY CLASSES

Digital System Design

B.Tech. 3rd Sem

EC & Allied



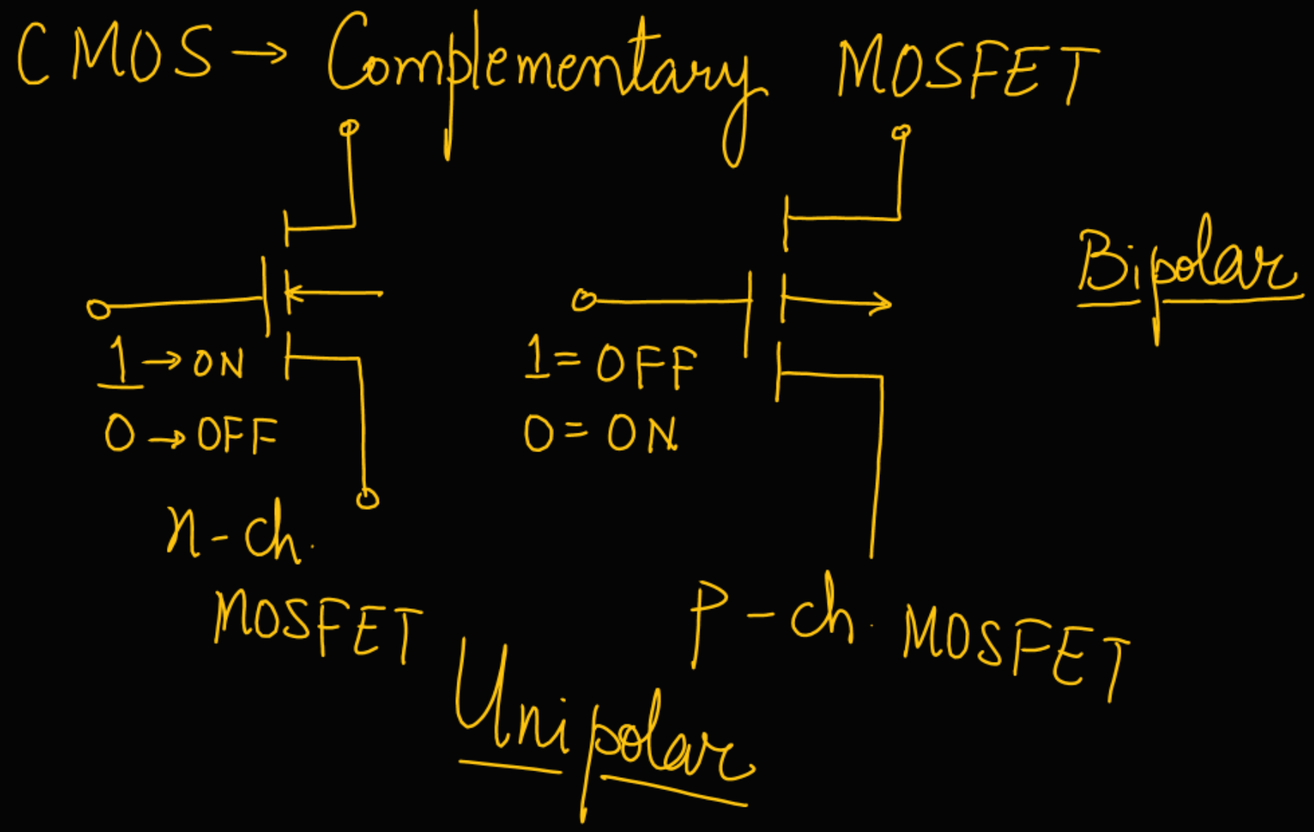
Exam/Result Oriented Content

- ✓ Recorded Video Lectures
- ✓ Pdf Notes
- ✓ PYQs

Lec 5

Today's Target

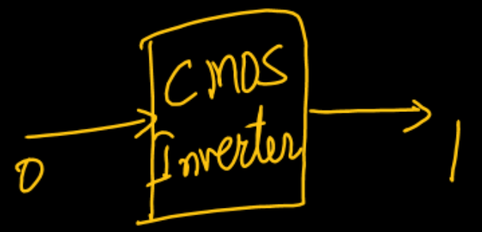
- CMOS Technology ✓
- CMOS Inverter ✓
- CMOS NAND Gate ✓
- CMOS AND Gate ✓
- CMOS NOR Gate ✓
- CMOS OR Gate ✓
- University Questions ✓



UNIVERSITY QUESTIONS

YEAR	QUESTIONS	MARKS
22-23 19-20	Describe figure of merit & noise immunity of TTL & CMOS ICs	2 Marks
22-23	Draw CMOS inverter circuit and explain its working.	10 Marks
21-22	Draw a circuit diagram of a CMOS inverter. Draw its transfer characteristics and explain its operation.	10 Marks
20-21	With the help of a neat diagram, explain the working of any two I. a CMOS inverter, II. a two input CMOS NAND gate III. a two input CMOS NOR gate	10 Marks
19-20	Compare TTL and CMOS logic families and also draw CMOS NOR gate.	10 Marks

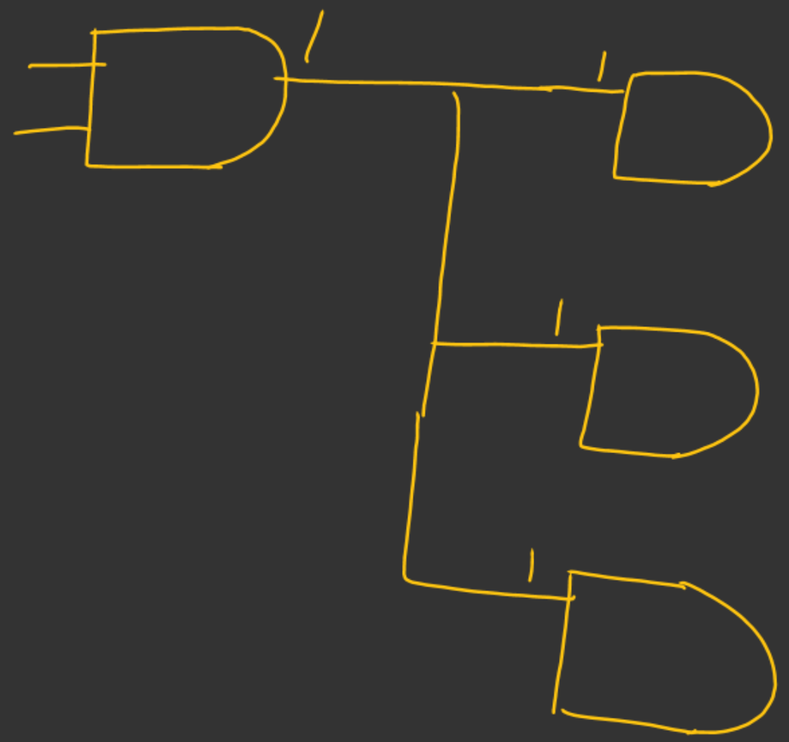
CMOS Technology



- Stands for "Complementary Metal Oxide Semiconductor."
- It is a technology used to produce integrated circuits.
- CMOS circuits are found in several types of electronic components, including microprocessors, batteries, and digital camera image sensors.
- Fabrication process that uses complementary and symmetrical pairs of p-type and n-type MOSFETs for logic functions.
- Two important characteristics of CMOS devices are high noise immunity and low static power consumption.
- Since one transistor of the MOSFET pair is always off, the series combination draws significant power only momentarily during switching between on and off states.
- CMOS devices do not produce as much waste heat as other forms of logic.
- These characteristics allow CMOS to integrate a high density of logic functions on a chip.
- The most widely used technology to be implemented in VLSI chips.

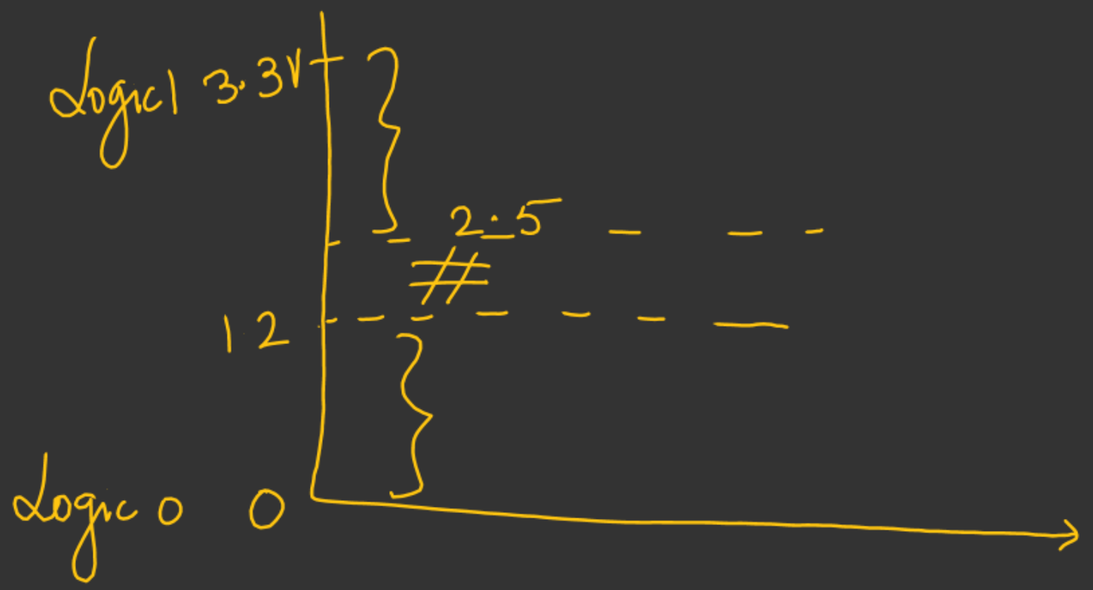
Difference between CMOS and TTL

Characteristics	CMOS	TTL
Voltage Levels	Wide range of voltage levels	Fixed voltage levels (typically 5V)
Power Consumption	Low	High
Technology	MOSFET	Bipolar Junction Transistor (BJT)
Noise Immunity	High	Low
Fan-Out Capability	High fan-out capability	Lower fan-out capability
Speed	Slow propagation delays	Fast propagation delays
Power Supply	Typically operates at 5V or 3.3V	Typically operates at 5V
Applications	Battery-operated devices, high-density ICs	High-speed applications, memory systems

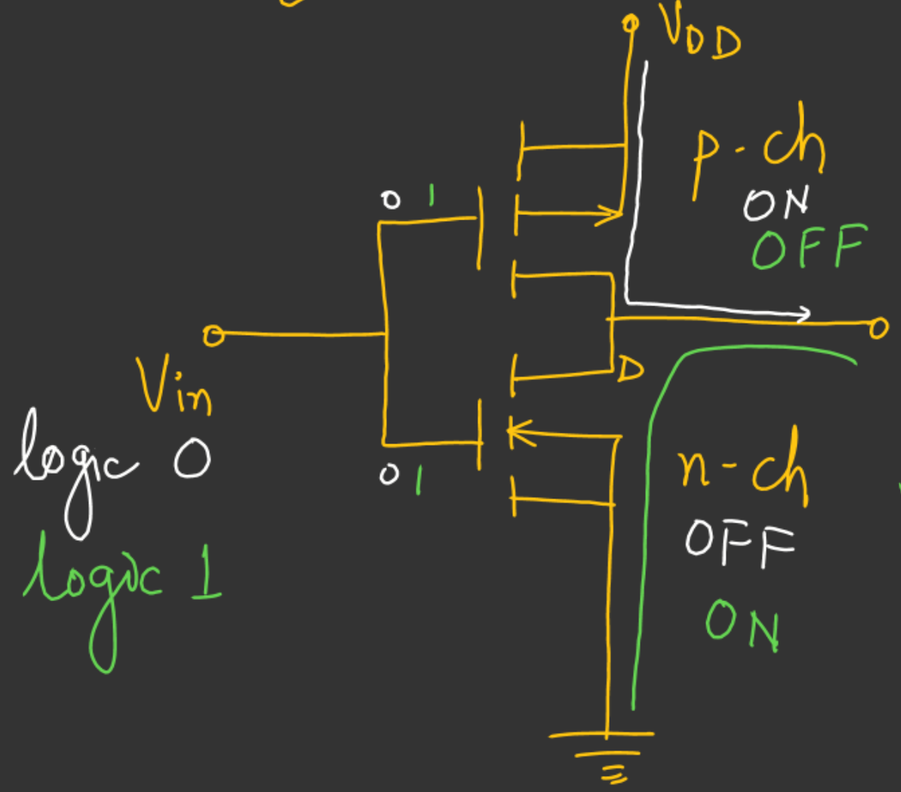


CMOS Inverter

- CMOS inverter are some of the most widely used and adaptable MOSFET inverters used in chip design.
- They operate with very little power loss and at relatively high speed.
- CMOS inverter has good logic buffer characteristics & its noise margins in both low and high states are large.
- A CMOS inverter contains a PMOS and a NMOS transistor connected at the drain and gate terminals, a supply voltage VDD at the PMOS source terminal, and a ground connected at the NMOS source terminal.
- V_{IN} is connected to the gate terminals and V_{OUT} is connected to the drain terminals.
- As the voltage at the input of the CMOS device varies between 0 and 5 volts, the state of the NMOS and PMOS varies accordingly.
- When V_{IN} is low, the NMOS is "off", while the PMOS stays "on": instantly charging V_{OUT} to logic high.
- When Vin is high, the NMOS is "on and the PMOS is "off" draining the voltage at V_{OUT} to logic low.


Logic1 3.3V
2.5
1.2
Logic 0
0

CMOS Inverter

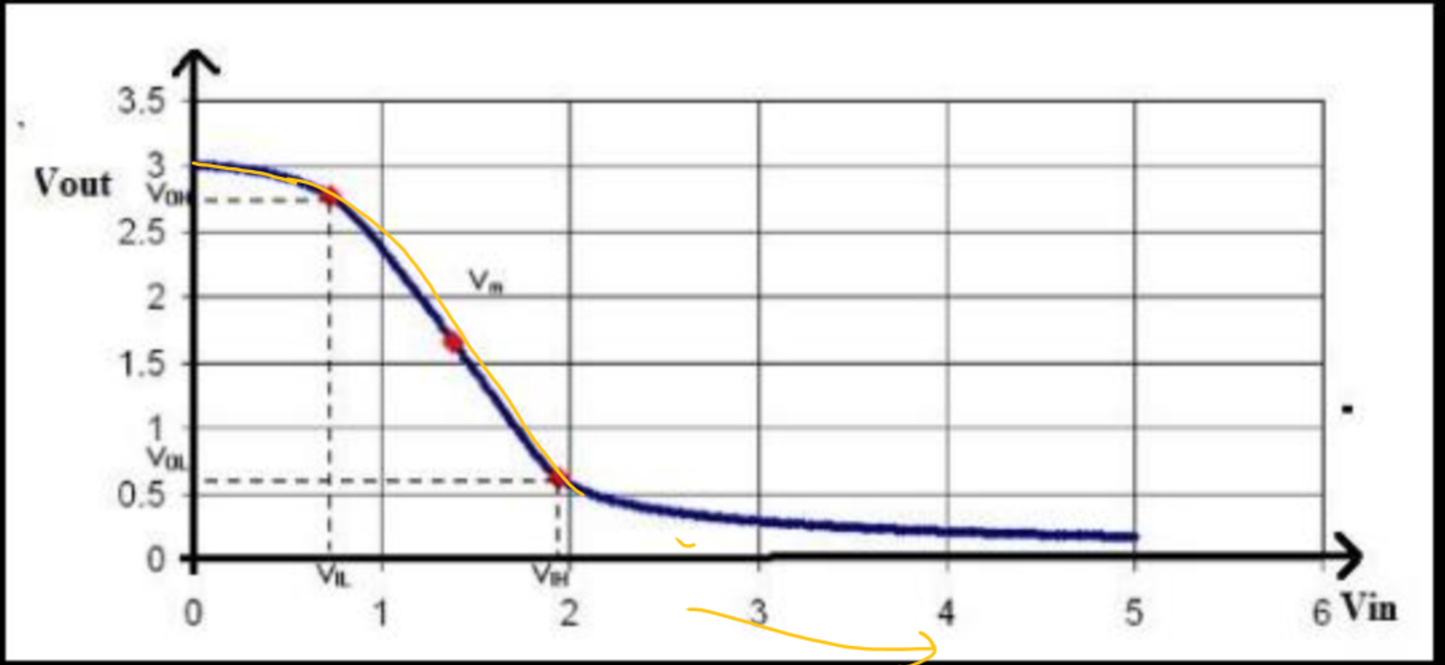


p-ch i/p = 0
⇒ ON

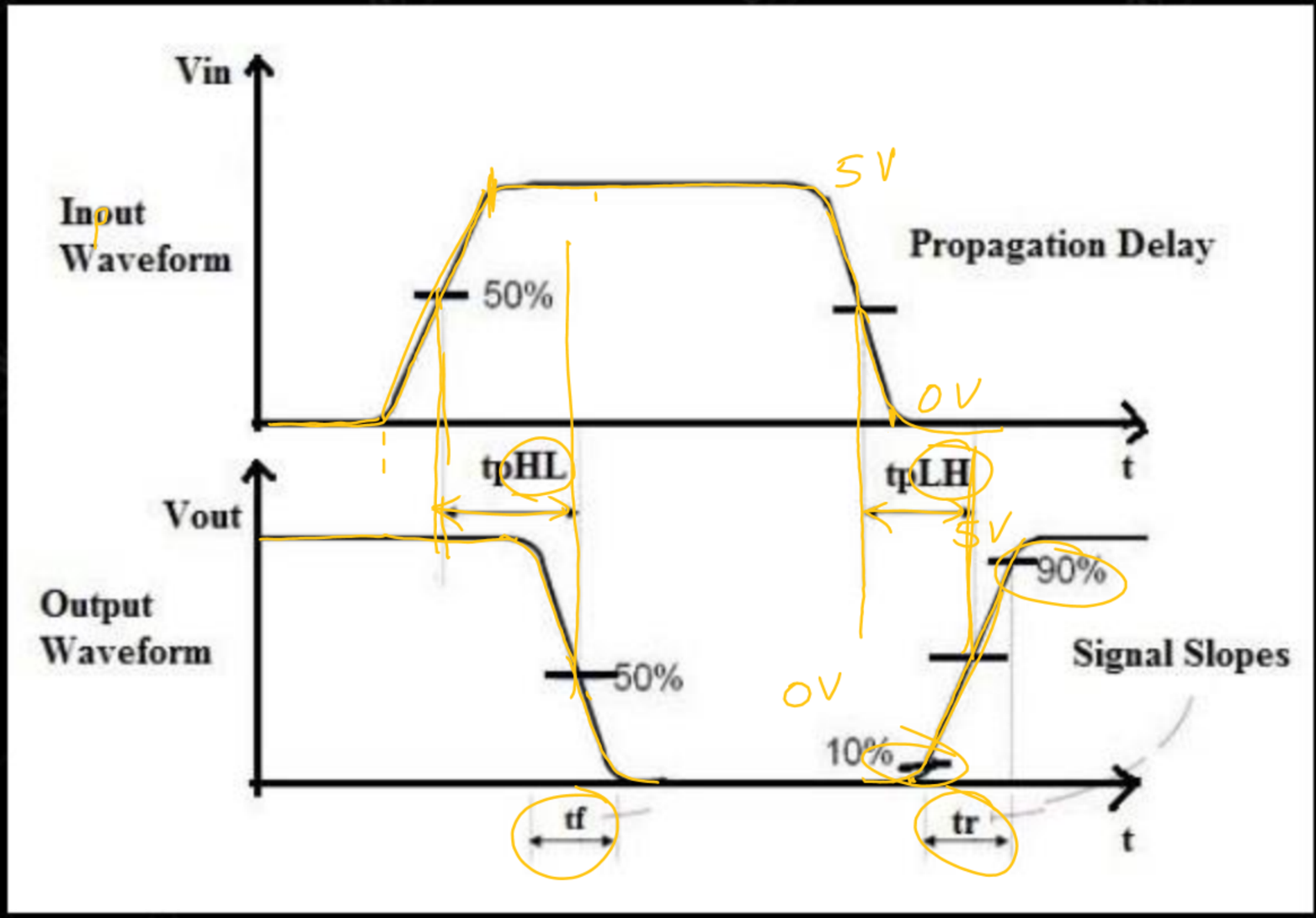
n-ch i/p = 1
⇒ ON

Inverter Static Characteristics or VTC

- The quality of the inverter can be measured frequently by using the VTC or voltage transfer curve, which is plotted between input voltage (Vin) and output voltage (Vo).
- From the following static characteristics, the parameters of devices like gain, operating logic levels & noise tolerance, and noise can be obtained.
- The transition region slope is a measure of quality – steep slopes yield exact switching.



Inverter Dynamic Characteristics



Inverter Dynamic Characteristics

- Rise Time or tr: Rise time is the time used to increase the signal from 10% to 90%.
- Fall Time or tf: Fall time is the time used to drop the signal from 90% to 10%
- Edge Rate or trf : It is (tr + tf)/2.
- The propagation delay from high to low or tpHL: The time used to drop from VOH – 50%.
- The propagation delay from low to high or tpLH: The time used to increase from 50%- VOL.
- Propagation Delay or tp: It is (tpHL + tpLH)/2.
- Contamination Delay or tcd: It is the smallest time from the 50% input crossing to the 50% output crossing.

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Advantages

- The CMOS inverter's steady-state power dissipation is negligible virtually, apart from small power dissipation because of leakage currents.
- The VTC (voltage transfer characteristic) exhibits a complete o/p voltage swing in between 0 V & VDD, and the transition of voltage transfer characteristic is normally very sharp. Thus, the characteristics of the CMOS inverter look like an ideal inverter.
- These inverters use electricity once they are switched ON & OFF resulting in less power consumption. As a result, these inverters generate extremely less waste heat to make them highly efficient, so used in small and delicate electronic devices.
- These inverters include high noise immunity, which lets them block both incoming & outgoing frequency spikes.
- These are low-cost to produce mass.

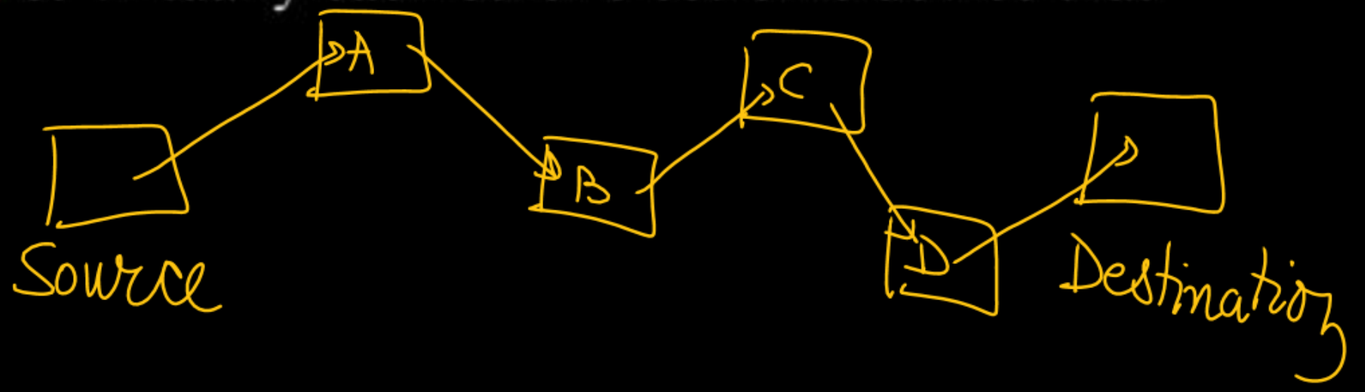
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Disadvantages

- As compared to other inverters, the switching speed of the CMOS inverter is high.
- These are very difficult to fabricate due to both the transistors used on the same Silica piece.
- It uses two transistors to make an inverter, so it uses more space on the IC as compared to the NMOS inverter.

Applications

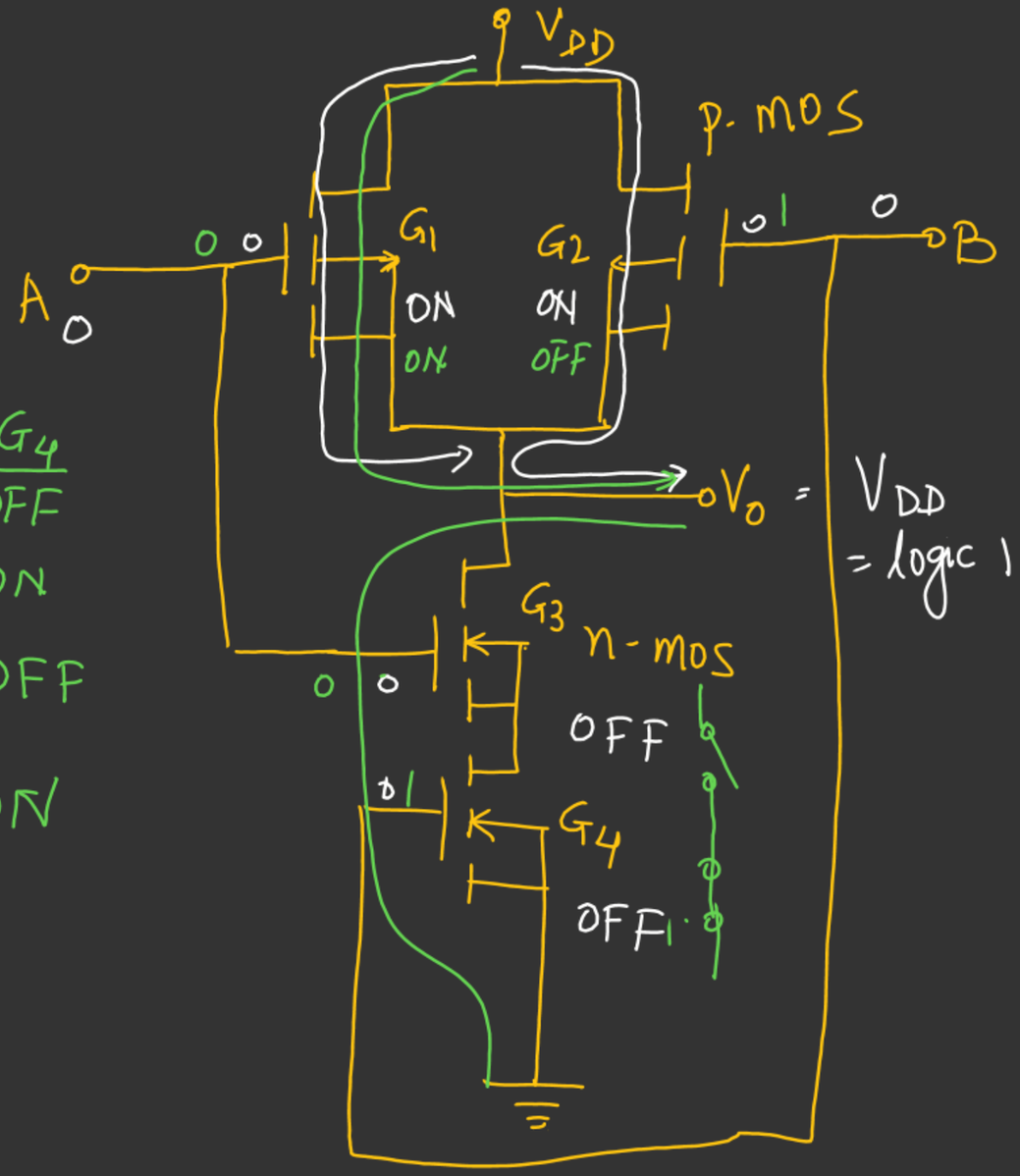
- CMOS inverters are used in different ICs (integrated circuits) like microprocessors, static RAM, microcontrollers, data converters, image sensors & transceivers.
- These are found in mobile devices, digital cameras, home computers, cell phones, routers, network servers, modems & virtually each other electronic device that needs logic functions.



CMOS NAND Gate

- It consists of two series NMOS transistors between Y and Ground and two parallel PMOS transistors between Y and V_{DD} .
- If either input A or B is logic 0, at least one of the NMOS transistors will be OFF, breaking the path from Y to Ground. But at least one of the PMOS transistors will be ON, creating a path from Y to V_{DD} . Hence, the output Y will be high.
- If both inputs are high, both of the NMOS transistors will be ON and both of the PMOS transistors will be OFF. Hence, the output will be logic low.

A	B	Pull Down network	Pull Up network	Output Y
0	0	OFF	ON	1
0	1	OFF	ON	1
1	0	OFF	ON	1
1	1	ON	OFF	0

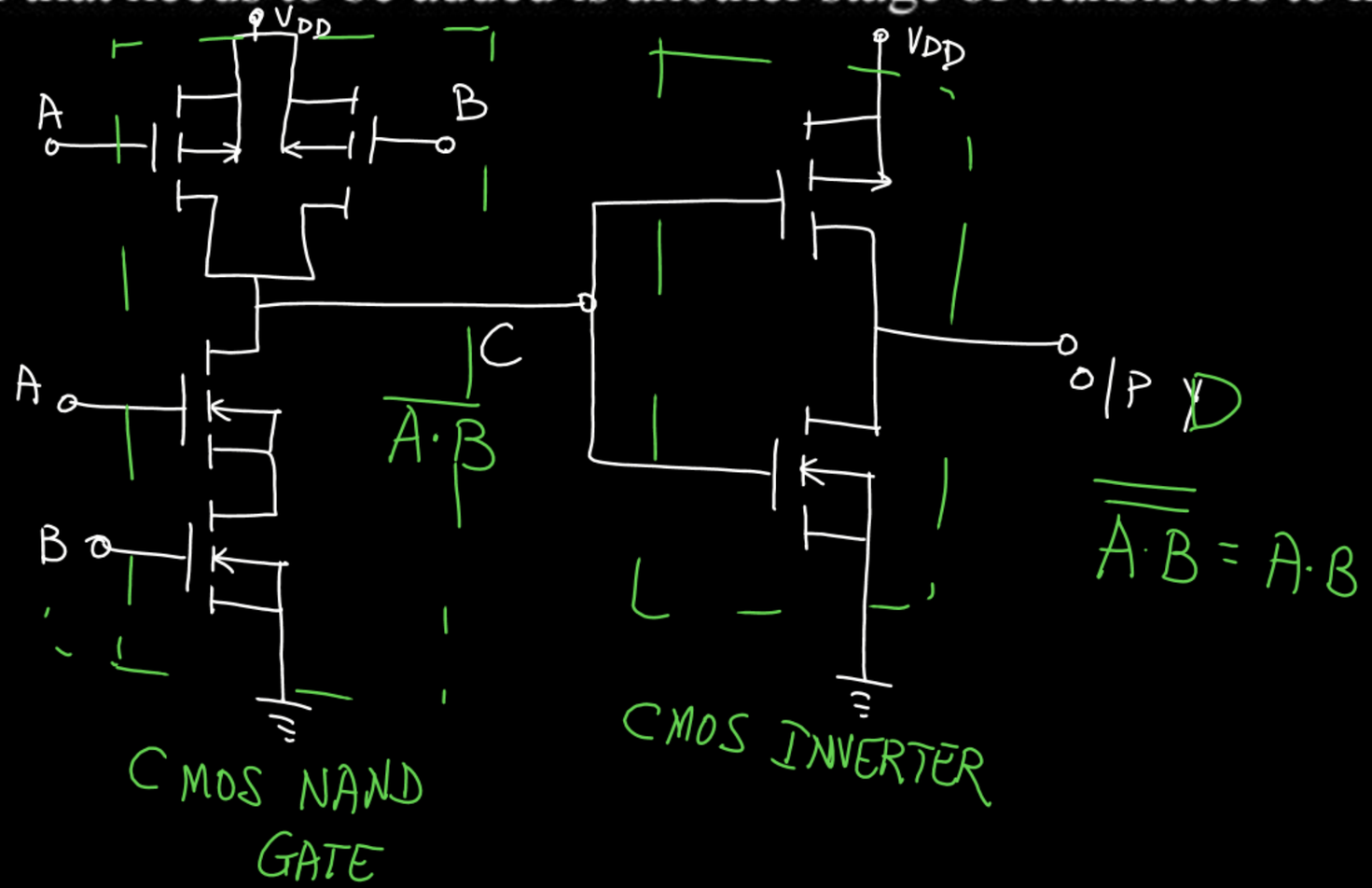


A	B	G_1	G_2	G_3	G_4
0	0	ON	ON	OFF	OFF
0	1	ON	OFF	OFF	ON
1	0	OFF	ON	ON	OFF
1	1	OFF	OFF	ON	ON

A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

CMOS AND Gate

- CMOS NAND gate circuit may be used as the starting point for the creation of an AND gate.
- All that needs to be added is another stage of transistors to invert the output signal.



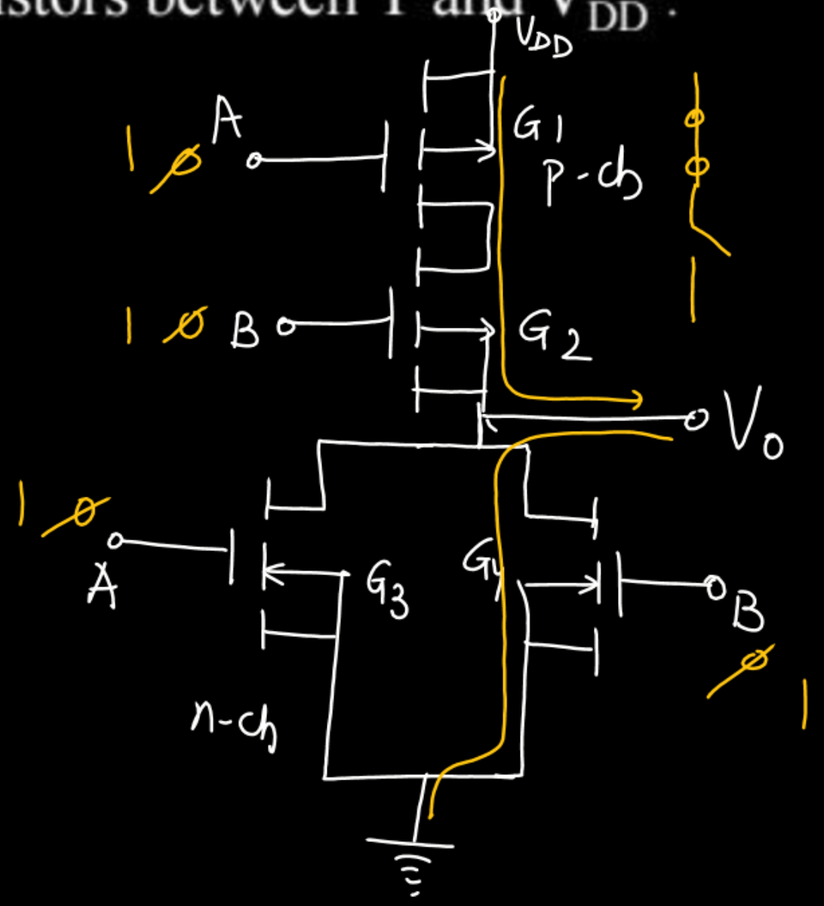
$\overline{A \cdot B} = A \cdot B$

AND

A	B	C	D
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

CMOS NOR Gate

- It consists of two paralle NMOS transistors between Y and Ground and two series PMOS transistors between Y and V_{DD} .



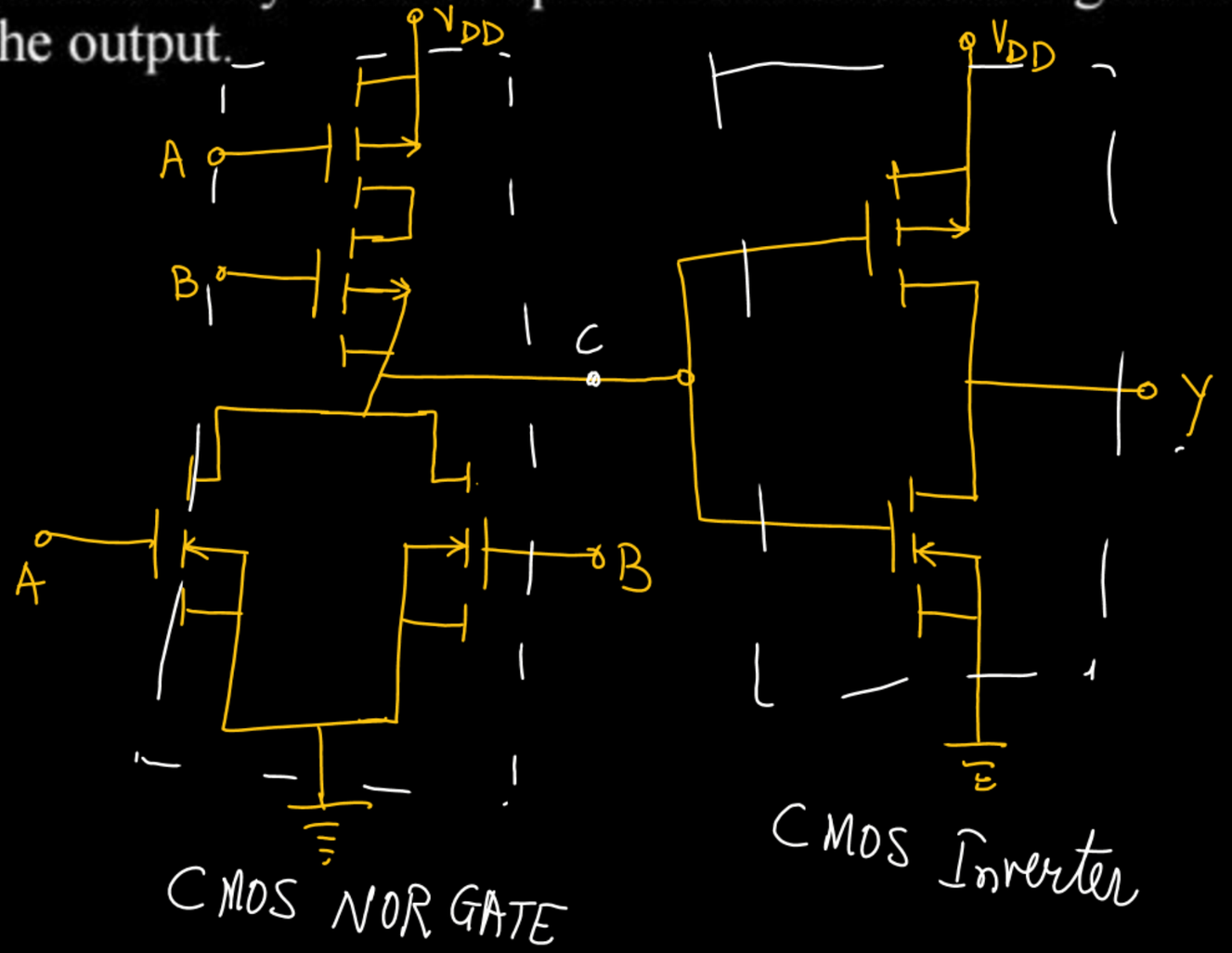
G_1	G_2	G_3	G_4
ON	ON	OFF	OFF
ON	OFF	OFF	ON
OFF	ON	ON	OFF
OFF	OFF	ON	ON

A	B	Output Y
0	0	1
0	1	0
1	0	0
1	1	0

$\overline{A+B}$

CMOS OR Gate

- The OR function may be built up from the basic NOR gate with the addition of an inverter stage on the output.

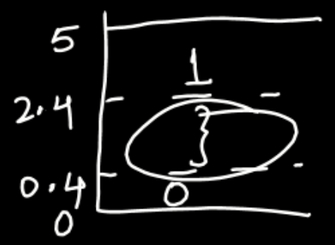


C	A	B	Output Y
1	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1

$\overline{A+B}$ $\overline{\overline{A+B}} = A+B$

Noise Immunity of TTL & CMOS ICs

- Digital logic requires specific voltages to be recognized as L or H.
  TTL voltage levels at 5V are:
- L - max 0.4V ✓
- H - min 2.4V



- CMOS at 5V requires:
- L - max 1.5V
- H - min 3.5V
- TTL on current side has better characteristics cause input currents are much higher:
- L - -1.6 mA ✓
- H - 40 uA ✓
- CMOS has very low input current in range of 100nA, 0.1uA.
- If input voltage is in-between then there is no guaranty which level will be recognized and logic gate might oscillate. In CMOS case both transistors might conduct what will increase power consumption. This also happens in case of slow slew rate input signal (current per pin is in range of few mA).

Figure of Merit

- The figure of merit of a digital IC is defined as the product of speed and power.
- The speed is specified in terms of propagation delay time expressed in nanoseconds.
- Figure of merit = propagation delay time (ns) x power (mW)
- It is specified in pico joules (ns x mW = pJ)

Specifications	TTL	CMOS
Basic Gate	NAND	NOR/NAND
Components	Passive Elements & Transistors	MOSFETs
Fan-out	10	>50
Noise Immunity	Strong	Extremely Strong
Noise Margin	Moderate	High
TPD in ns	1.5 to 30	1 to 210
Clock Rate in MHz	35	10
Power/Gate in mWatt	10	0.0025
Figure of Merit	100	0.7

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Thank You