AKTU

GATEWAY CLASSES

Digital System Design

B.Tech. 3rd Sem

EC & Allied



Exam/Result Oriented Content

- ✓ Recorded Video Lectures
- ✓ Pdf Notes
- ✓ PYQs

DIGITAL SYSTEM DESIGN

UNIT 4 : Logic families and semiconductor memories

Lec 6

Today's Target

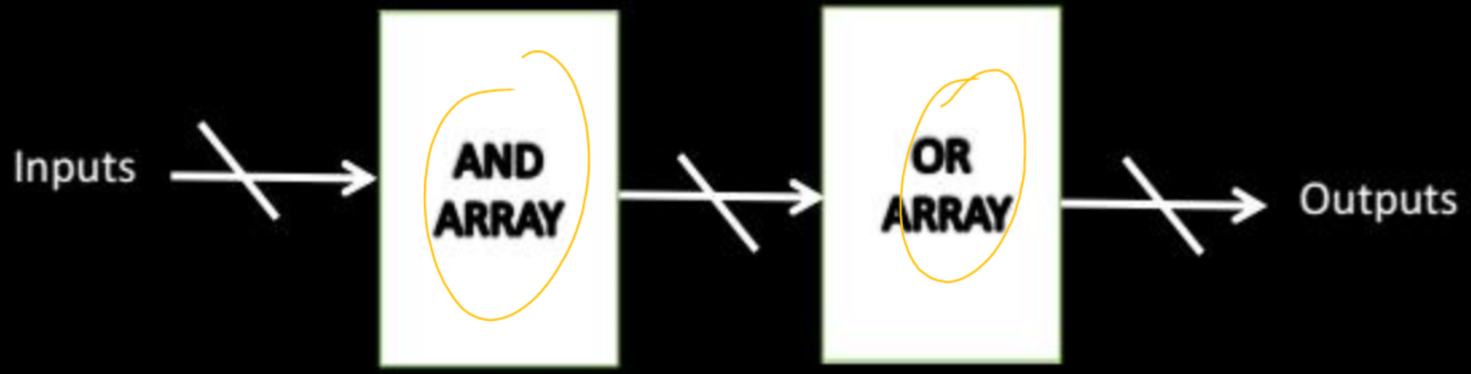
- Programmable Logic Devices (PLDs)
- Advantages of using PLDs
- fundamental types of standard PLDs
- **The ROM or PROM**
- The PLA
- The PAL
- University Questions

UNIVERSITY QUESTIONS

YEAR	QUESTIONS	MARKS
22-23 19-20	Define PLD's. Implement the following function using PLA $F1 = \Sigma m(0,3,4,7)$ $F2 = \Sigma m(1,2,5,7)$	10 Marks
18-19	Differentiate between PLA and PAL. Realize the full adder circuit using PAL.	7 Marks
18-19	Tabulate the truth table for 8x4 ROM that implements the Boolean function: $A(x, y, z) = \sum(1, 2, 4, 6)$ $B(x, y, z) = \sum(0, 1, 6, 7)$ $C(x, y, Z) = \sum(2, 6)$ $D(x, y, z) = \sum(1, 2, 3, 5, 7)$	7 Marks

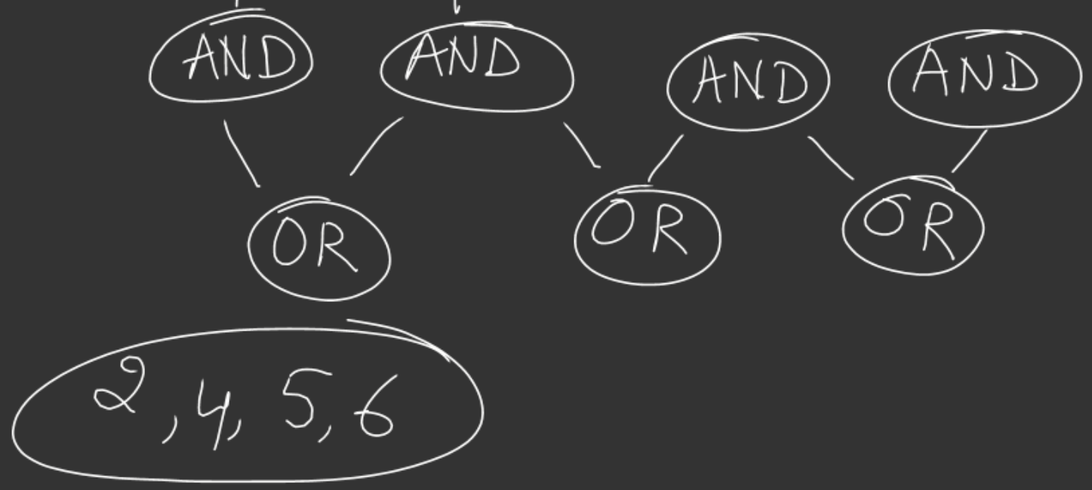
Programmable Logic Devices (PLDs)

- An IC that contains large numbers of gates, flip-flops, etc. that can be configured by the user to perform different functions is called a Programmable Logic Device (PLD).
- The internal logic gates and/or connections of PLDs can be changed/configured by a programming process.
- One of the simplest programming technologies is to use fuses.
- In the original state of the device, all the fuses are intact.
- Programming the device involves blowing those fuses along the paths that must be removed in order to obtain the particular configuration of the desired logic function.
- PLDs are typically built with an array of AND gates (AND-array) and an array of OR gates (OR-array).



SOP: $y = \sum m(0, 1, 3, 7)$

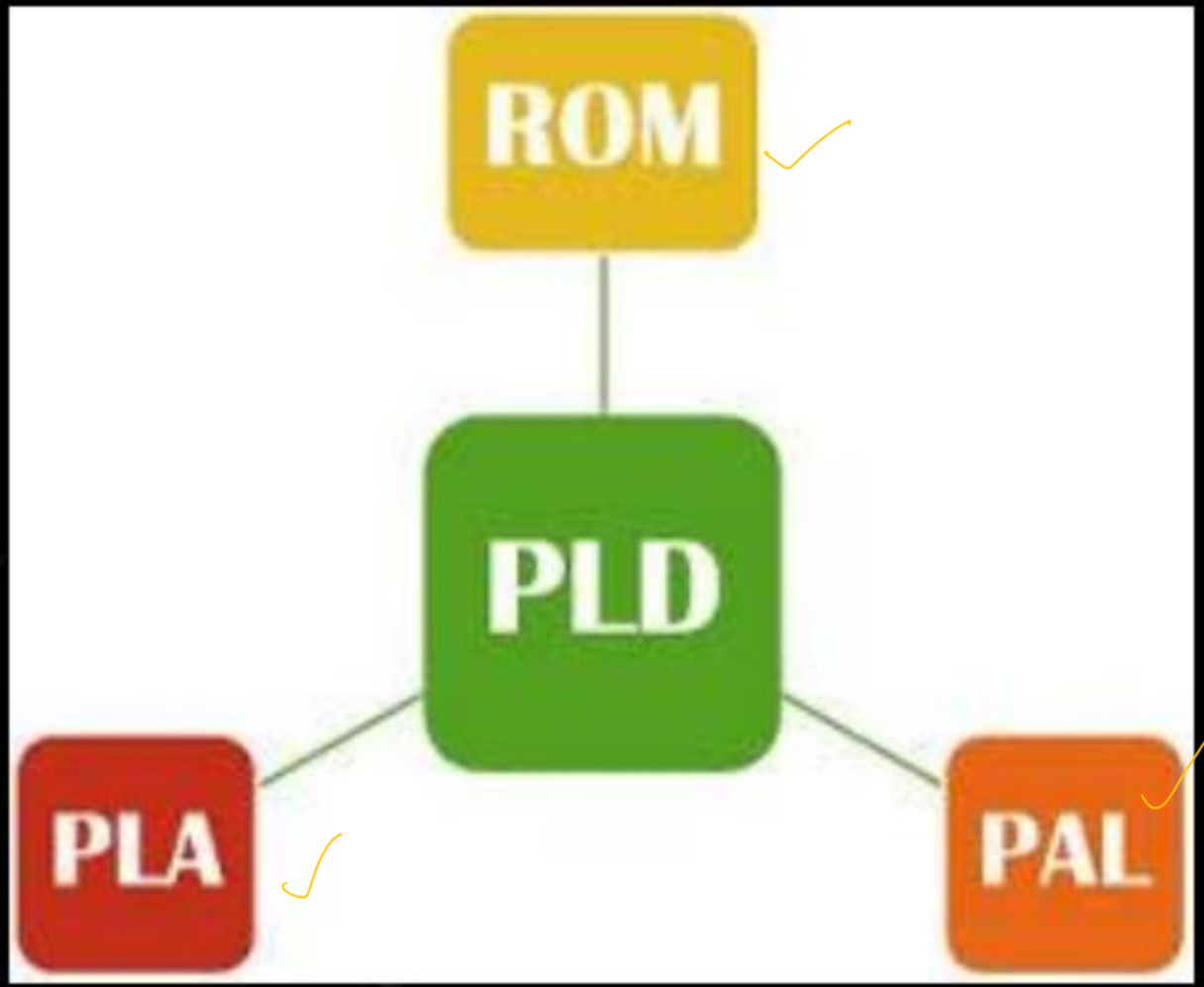
$= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}BC + ABC$



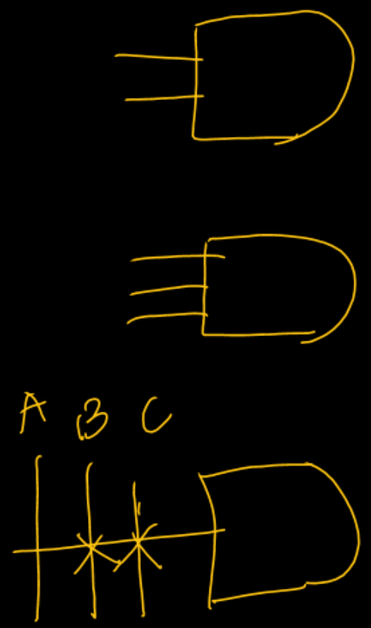
Advantages of using PLDs:

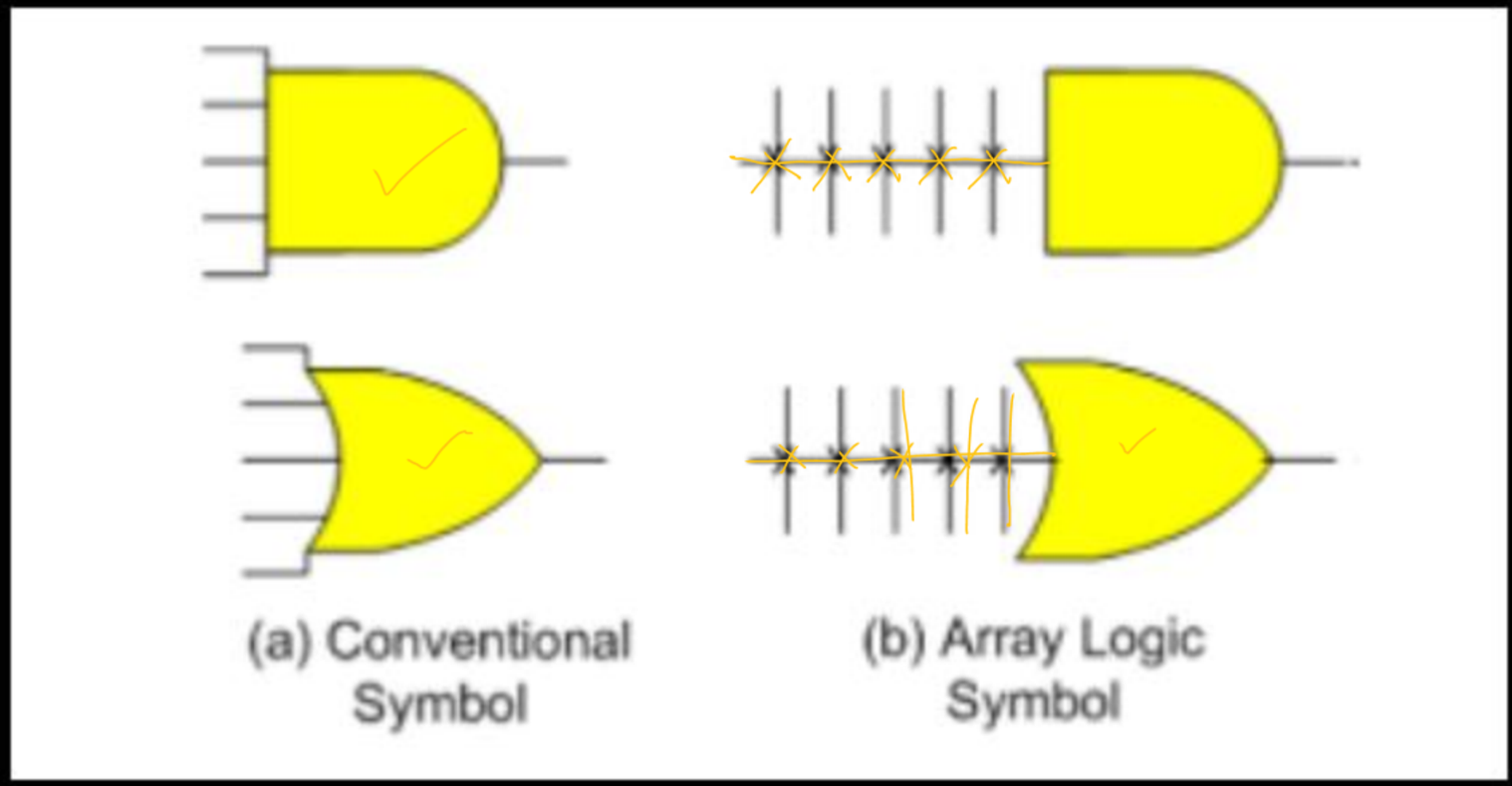
Problems of using standard ICs:	Advantages of using PLDs:
they require hundreds or thousands of these Ics	lower power requirements (i.e., smaller power supplies)
considerable amount of circuit board space	less board space
a great deal of time and cost in inserting, soldering, and testing.	faster
Also require keeping a significant inventory of ICs.	less costly assembly processes
	higher reliability (fewer ICs and circuit connections means easier troubleshooting)
	availability of design software.

Three fundamental types of standard PLDs



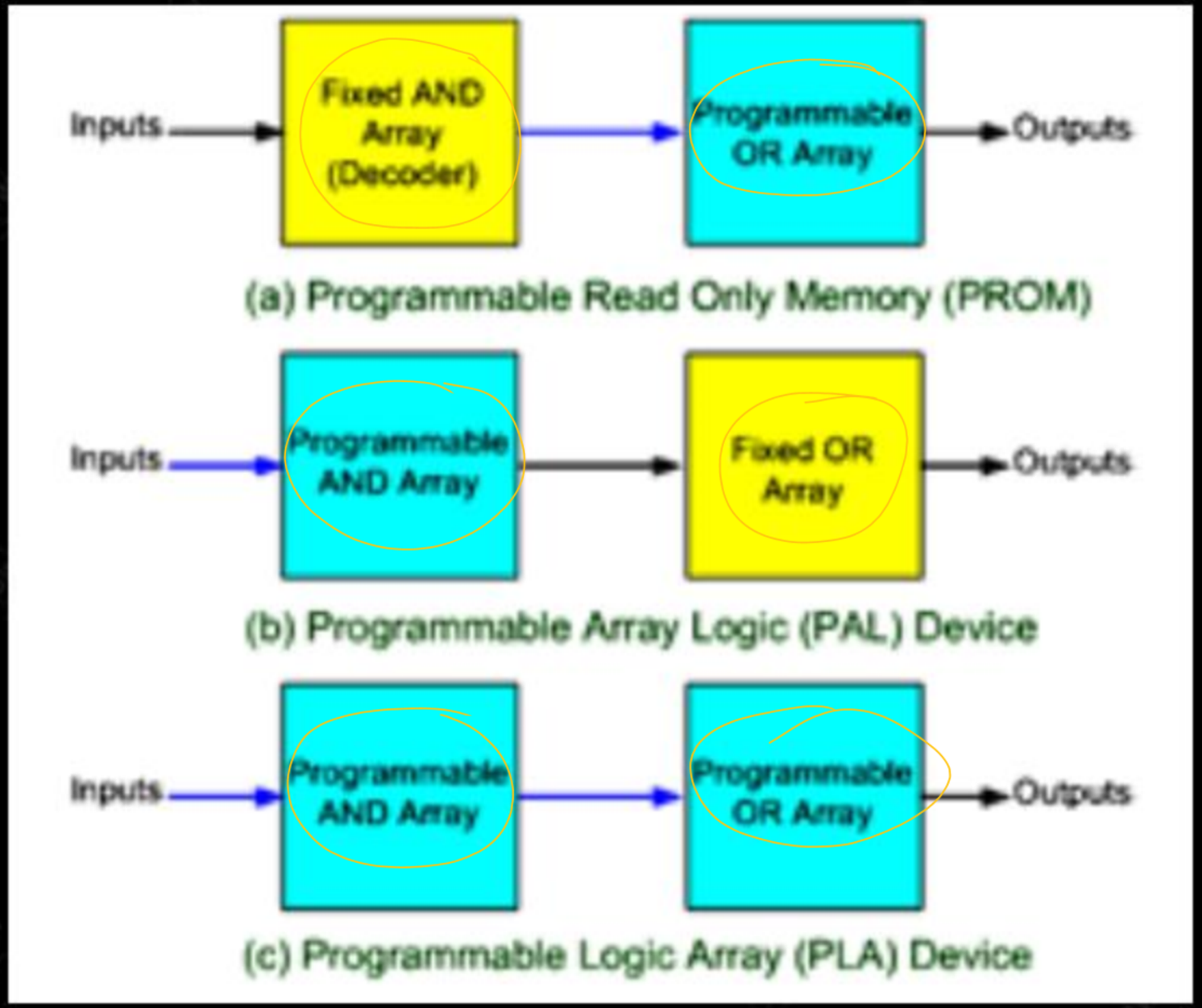
Conventional and Array Logic Symbols





Three Fundamental Types of PLDs:

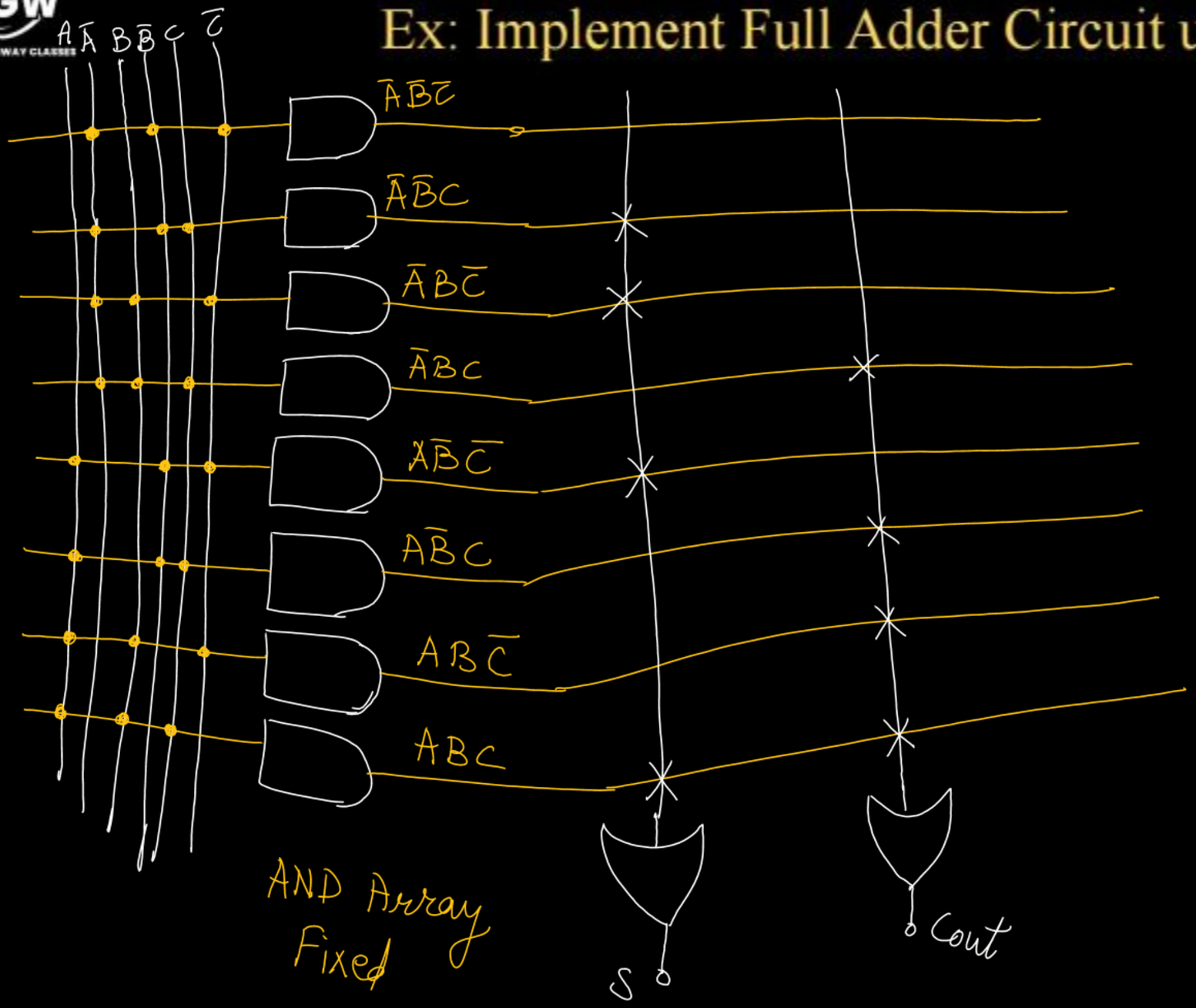
- The PROM (Programmable Read Only Memory) has a fixed AND array (constructed as a decoder) and programmable connections for the output OR gates array. The PROM implements Boolean functions in sum-of-minterms form.
- The PAL (Programmable Array Logic) device has a programmable AND array and fixed connections for the OR array.
- The PLA (Programmable Logic Array) has programmable connections for both AND and OR arrays. So it is the most flexible type of PLD.


Inputs
Fixed AND Array (Decoder)
Programmable OR Array
Outputs
(a) Programmable Read Only Memory (PROM)
Inputs
Programmable AND Array
Fixed OR Array
Outputs
(b) Programmable Array Logic (PAL) Device
Inputs
Programmable AND Array
Programmable OR Array
Outputs
(c) Programmable Logic Array (PLA) Device

The ROM (Read Only Memory) or PROM (Programmable Read Only Memory):

- The input lines to the AND array are hard-wired
- the output lines to the OR array are programmable.
- Each AND gate generates one of the possible AND products (i.e., minterms).

Ex: Implement Full Adder Circuit using PROM.



A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$S = \Sigma m(1, 2, 4, 7)$

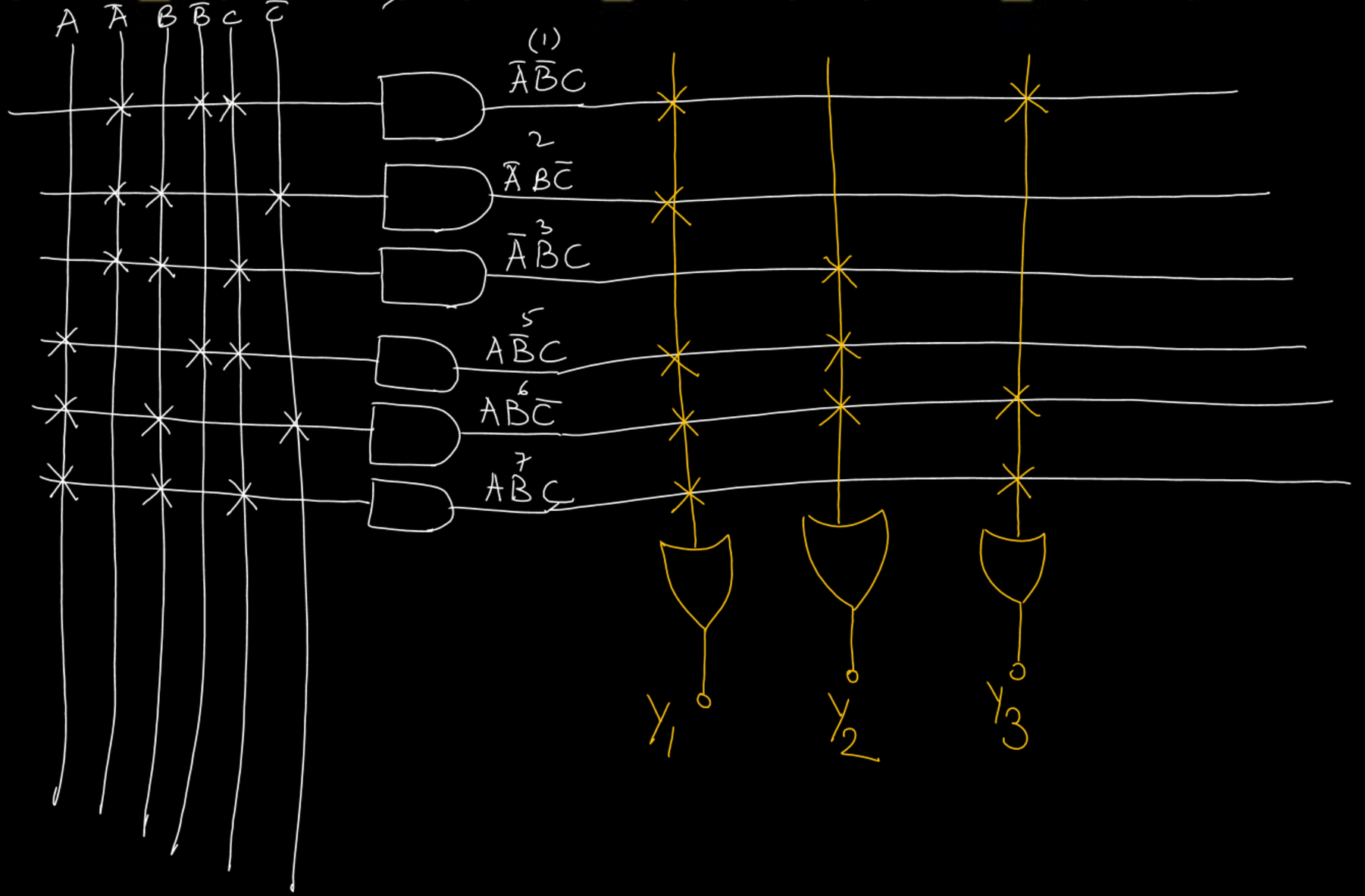
$Cout = \Sigma m(3, 5, 6, 7)$

The PLA (Programmable Logic Array):

- Each of the AND gates can be programmed to generate a product term of the input variables and does not generate all the minterms as in the ROM.
- The AND and OR gates inside the PLA are initially fabricated with the links (fuses) among them.
- It consists of n inputs, m outputs, and k product terms.
- The product terms constitute a group of k AND gates each of 2n inputs.
- Links are inserted between all n inputs and their complement values to each of the AND gates.
- Links are also provided between the outputs of the AND gates and the inputs of the OR gates.
- PLA has m-outputs, the number of OR gates is m.

Ex: Implement the following boolean function using PLA:

a) $Y1 = \sum m(1,2,5,6,7)$ b) $Y2 = \sum m(3,5,6)$ c) $Y3 = \sum m(1,6,7)$



The PAL (Programmable Array Logic):

- The PAL device is a PLD with a fixed OR array and a programmable AND array.
- PAL device is easier to program but it is not as flexible as the PLA.

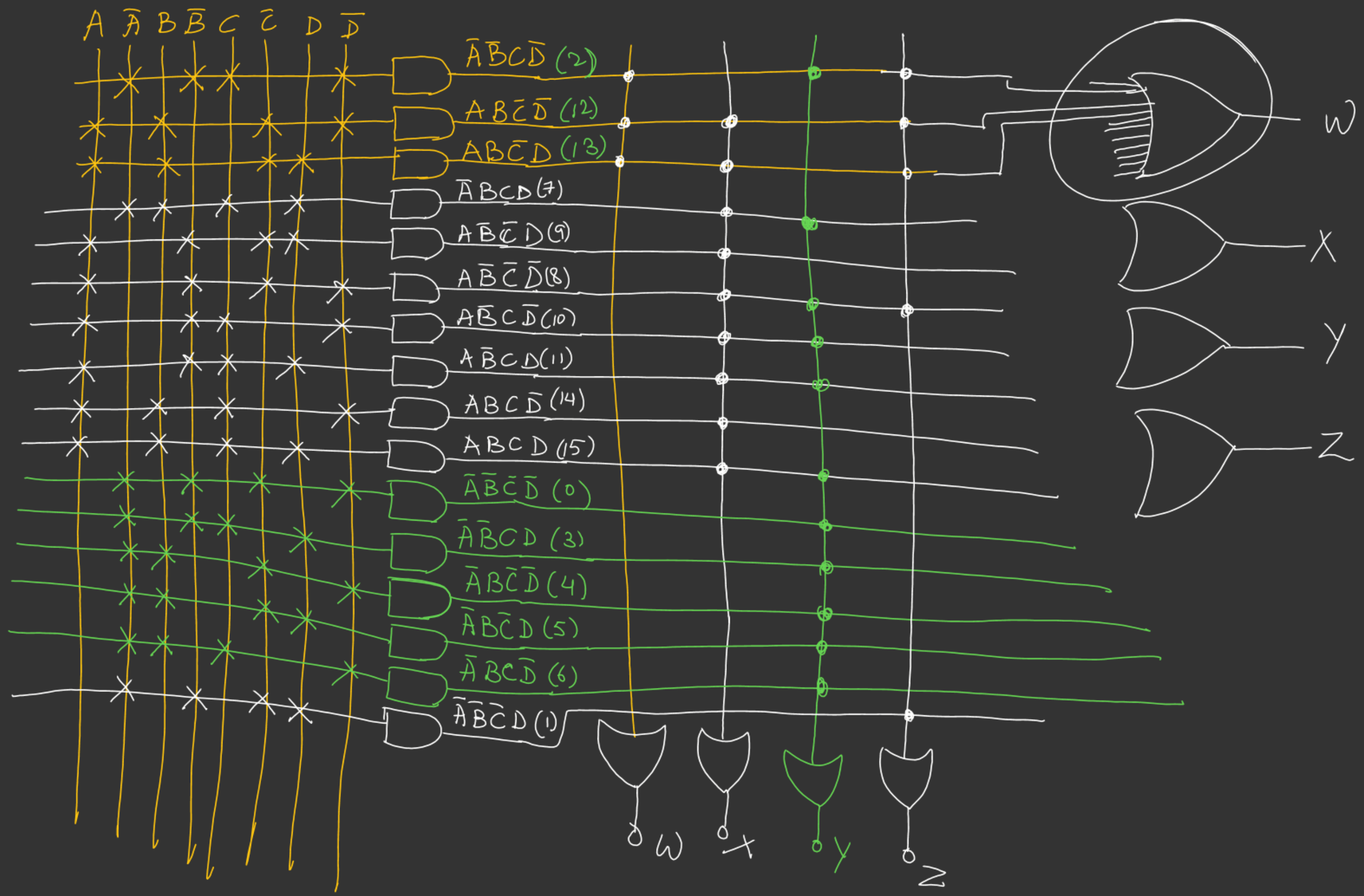
Example: Implement the following Boolean functions using the PAL device

$W(A, B, C, D) = \sum m(2, 12, 13)$

$X(A, B, C, D) = \sum m(7, 8, 9, 10, 11, 12, 13, 14, 15)$

$Y(A, B, C, D) = \sum m(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)$

$Z(A, B, C, D) = \sum m(1, 2, 8, 12, 13)$


A Ā B B̄ C C̄ D D̄
ĀB̄CD̄ (2)
AB̄C̄D̄ (12)
AB̄CD (13)
ĀBCD (7)
AB̄C̄D (9)
AB̄C̄D̄ (8)
AB̄CD̄ (10)
ĀBC̄D (11)
ABCD̄ (14)
ABCD (15)
ĀB̄C̄D̄ (0)
ĀB̄CD (3)
ĀB̄C̄D̄ (4)
ĀB̄C̄D (5)
ĀBCD̄ (6)
ĀB̄CD (1)
W
X
Y
Z
W
X
Y
Z

GATEWAY CLASSES

AKTU Full Courses (Paid)

Download Gateway Classes Application

From Google Play store

All Subjects

Link in Description

Thank You