AKTU

GATEWAY CLASSES

Digital System Design

B.Tech. 3rd Sem

EC & Allied



Exam/Result Oriented Content

- ✓ Recorded Video Lectures
- ✓ Pdf Notes
- ✓ PYQs

DIGITAL SYSTEM DESIGN

UNIT 3 : Sequential logic design
Lec 4

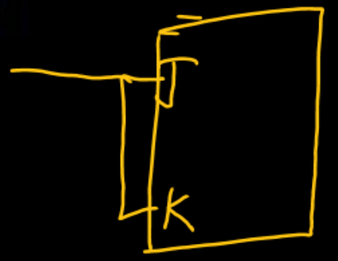
Today's Target

- Counters
- Asynchronous or Ripple Counters (UP & DOWN Counter)
- Synchronous counters (UP & DOWN Counter)
- University Questions

UNIVERSITY QUESTIONS

YEAR	QUESTIONS	MARKS
21-22	Write the difference between ripple counter and synchronous counter	5 Marks
20-21	Design and implement a synchronous 3-bit up/down counter using JK flip-flops.	10 Marks
18-19	Design a ripple decade counter using JK flip	7 Marks

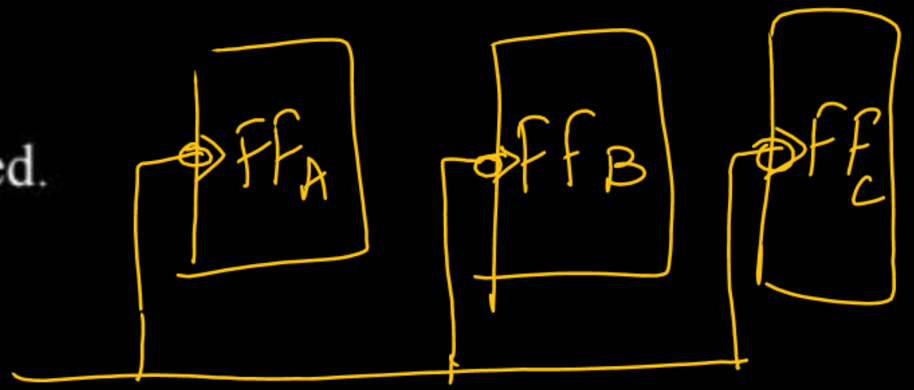
Counters



- Counter is a sequential circuit.
- A digital circuit which is used for a counting pulses is known counter.
- Counter is the widest application of flip-flops.
- It is a group of flip-flops with a clock signal applied.
- Counters are of two types.

1) Asynchronous or ripple counters. ✓

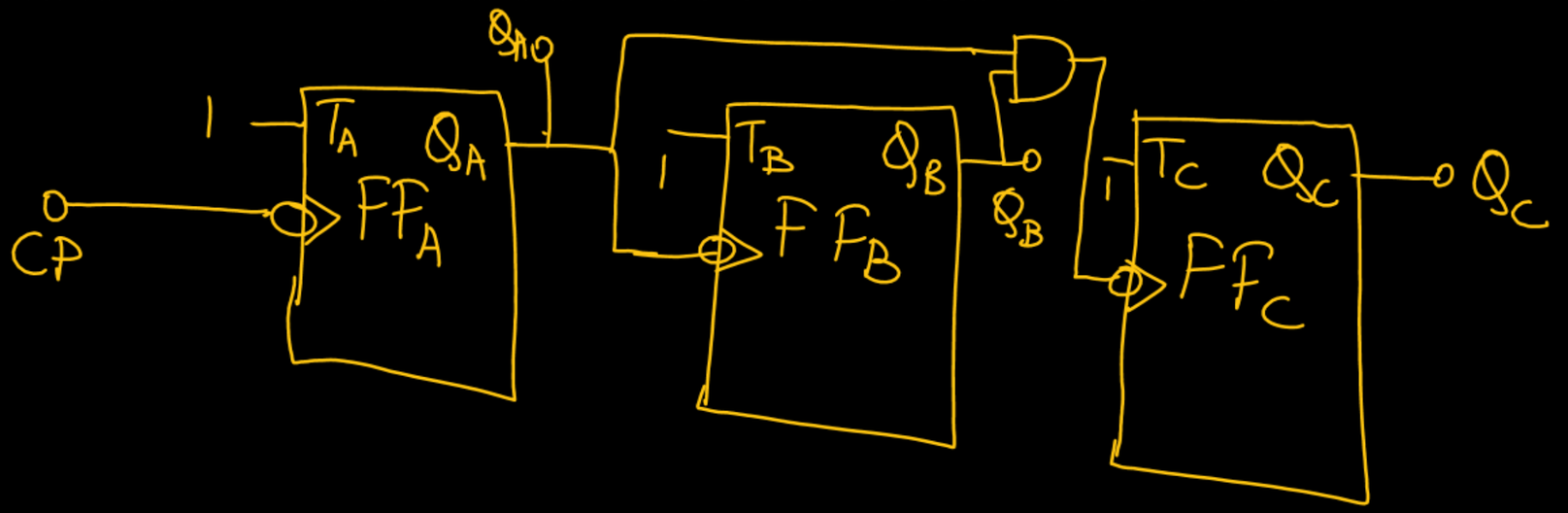
2) Synchronous counters. ✓





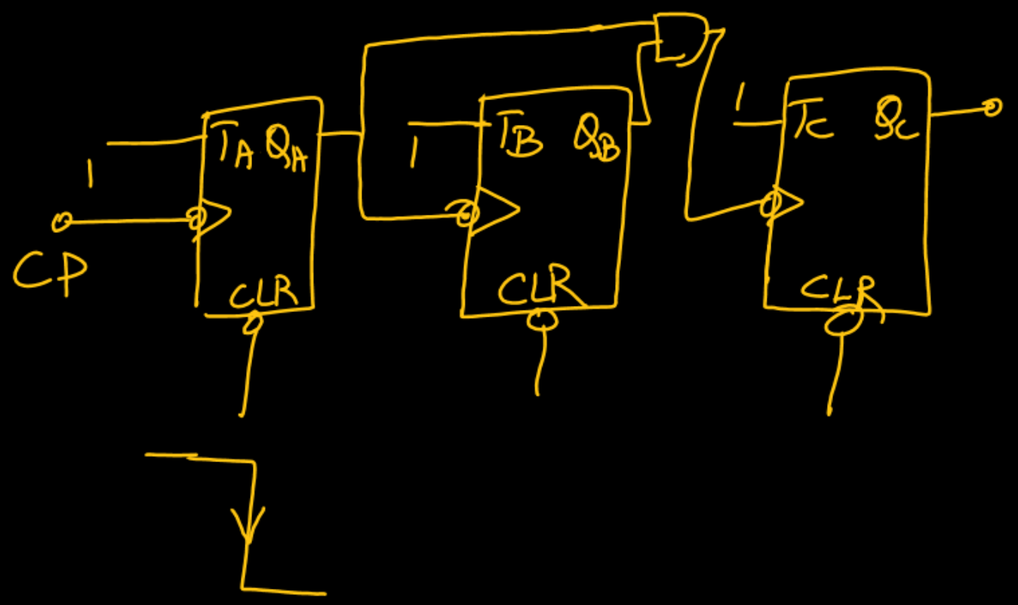
Asynchronous or Ripple Counters

- The toggle (T) flip-flop are being used.
- External clock is applied to the clock input of flip-flop A and QA output is applied to the clock input of the next flip-flop i.e. FF-B and QB output is applied to the clock input of the next flip-flop i.e. FF-C
- The logic diagram of a 3-bit ripple up counter is shown below.

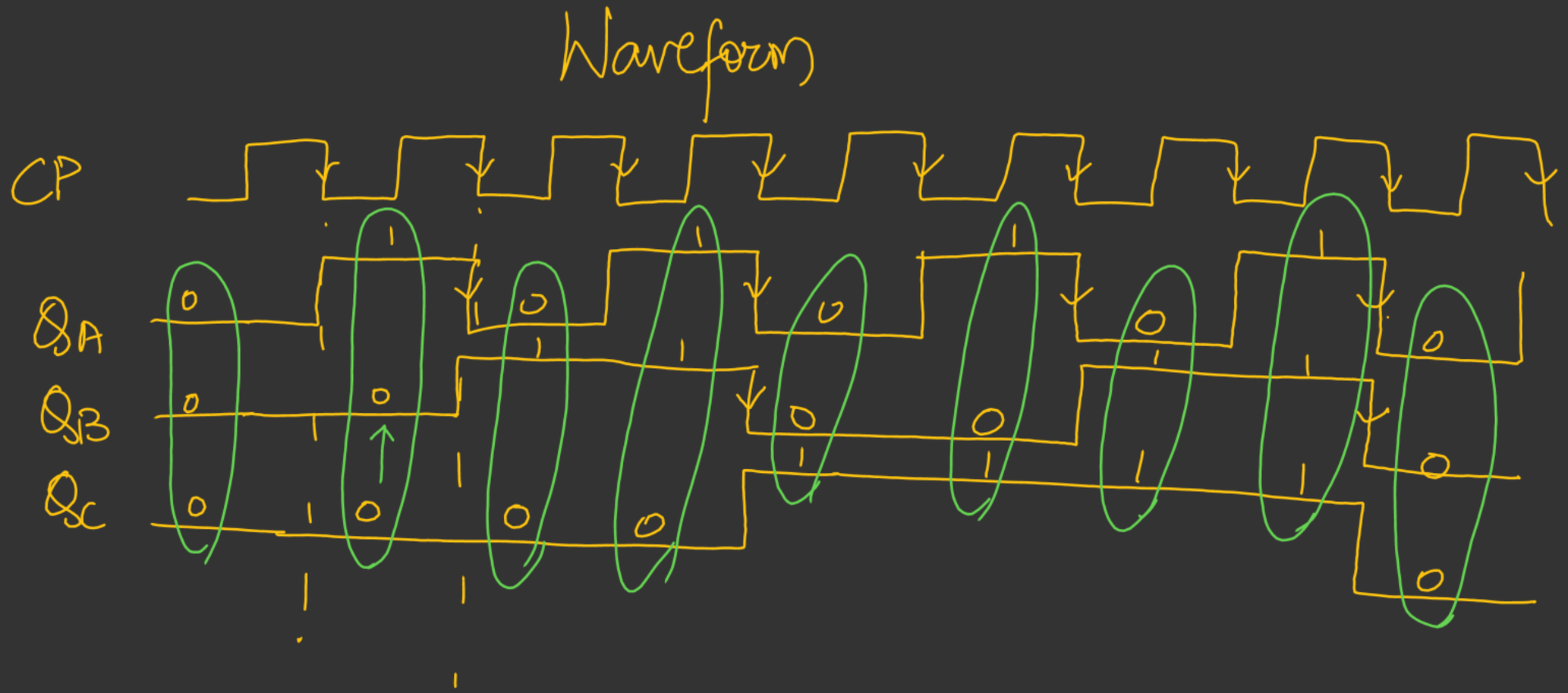


Truth Table

CLK	Counter Output			State Number	Decimal Number
	QC	QB	QA		
Initially	0	0	0	1	0
1st	0	0	1	2	1
2nd	0	1	0	3	2
3rd	0	1	1	4	3
4th	1	0	0	5	4
5th	1	0	1	6	5
6th	1	1	0	7	6
7th	1	1	1	8	7
8th	0	0	0	1	0

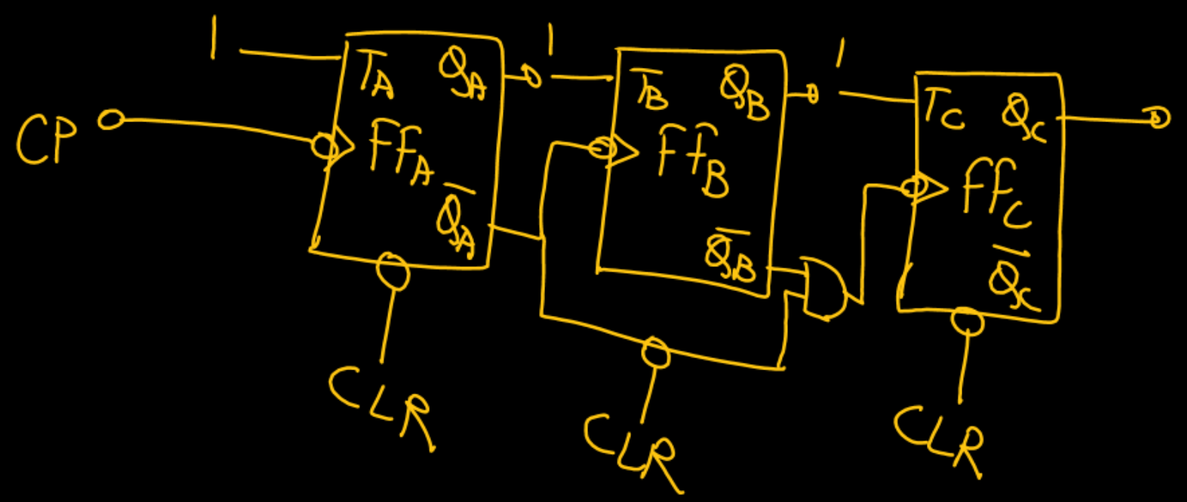


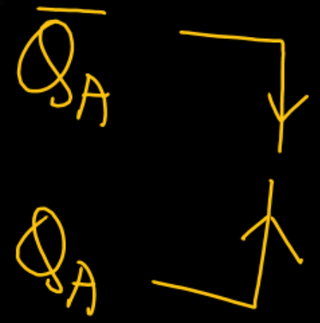
Waveform

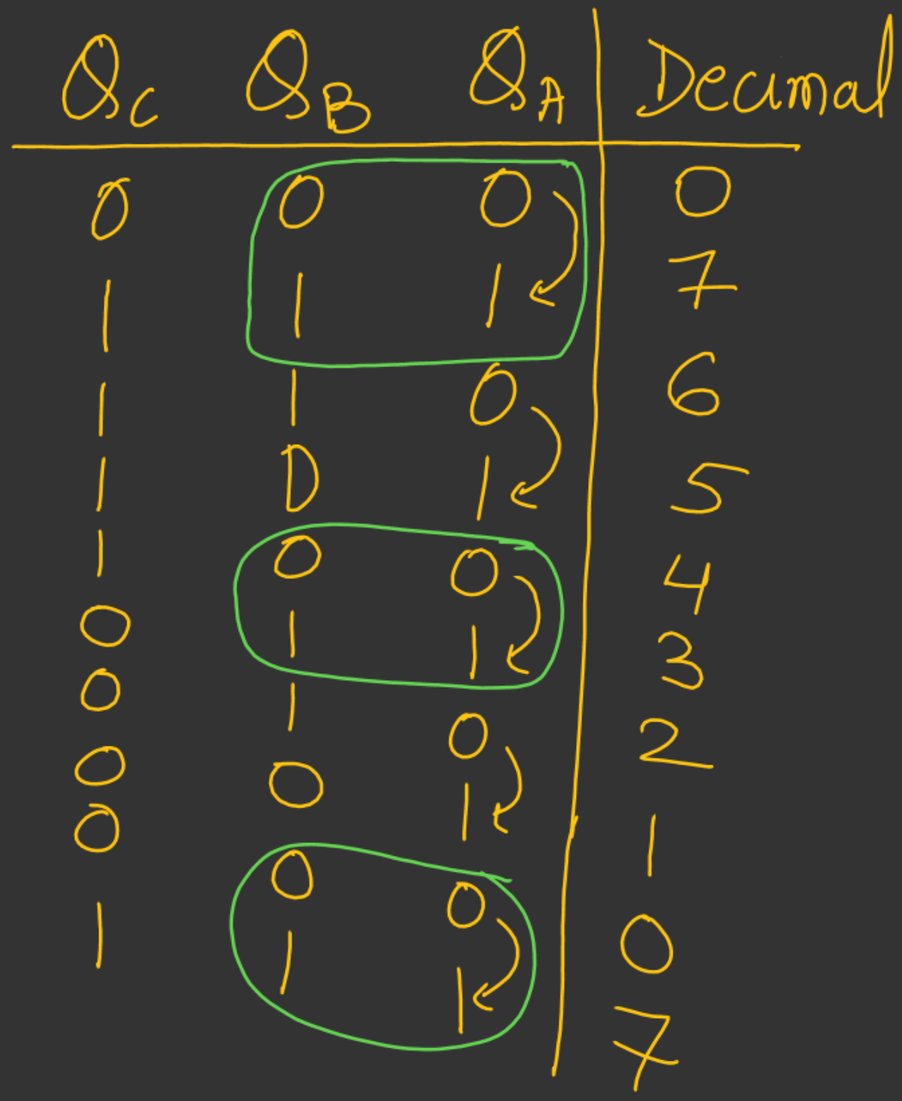


Asynchronous Binary Down Counter

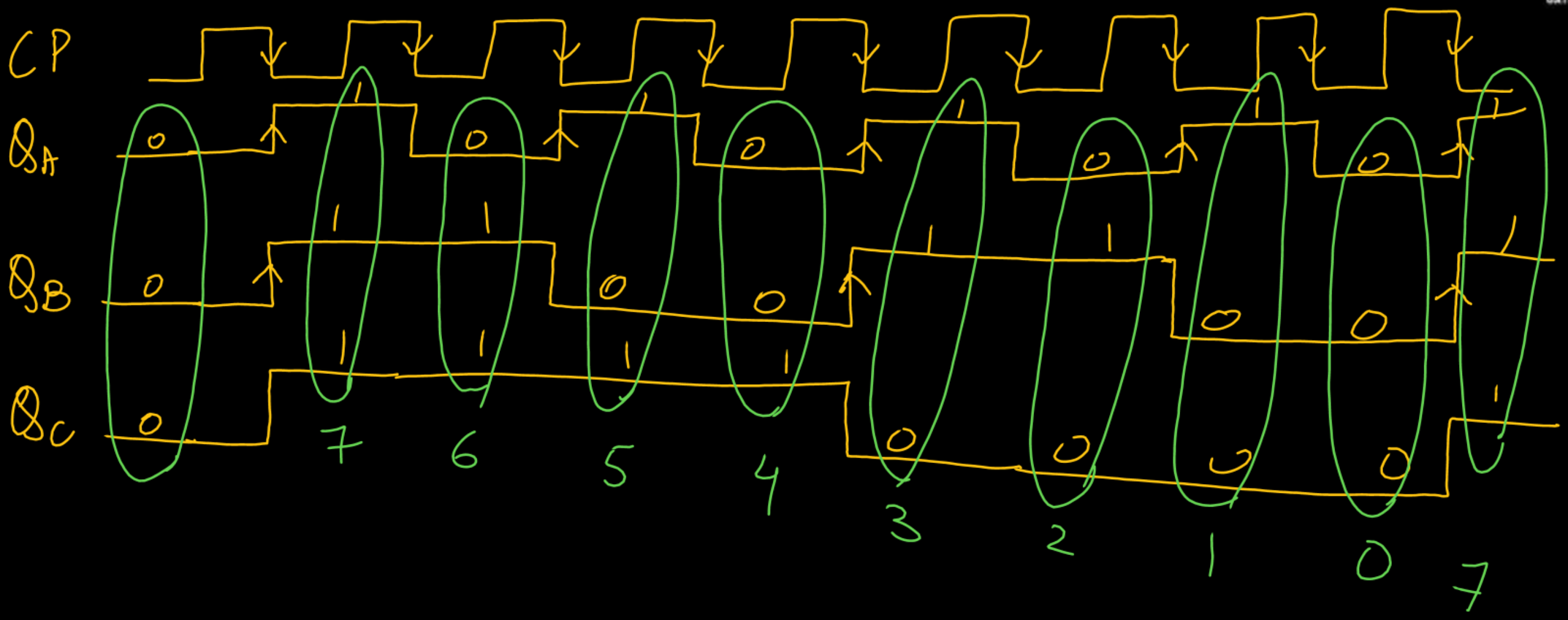
- consists of 'N' T flip-flops.
- It counts from $2^N - 1$ to 0.
- The block diagram of 3-bit Asynchronous binary down counter is shown in the following figure.
- Assume the initial status of T flip-flops from rightmost to leftmost is Q2Q1Q0=000
- Q0 toggled for every negative edge of clock signal.
- Q1 toggles when Q0 goes from 0 to 1, otherwise remained in the previous state.
- Q2 toggles when Q1 that goes from 0 to 1, otherwise remained in the previous state.






Q_C Q_B Q_A Decimal
0 0 0 0
0 1 1 7
1 1 0 6
1 0 1 5
1 0 0 4
0 1 1 3
0 1 0 2
0 0 1 1
1 0 0 0
1 1 1 7

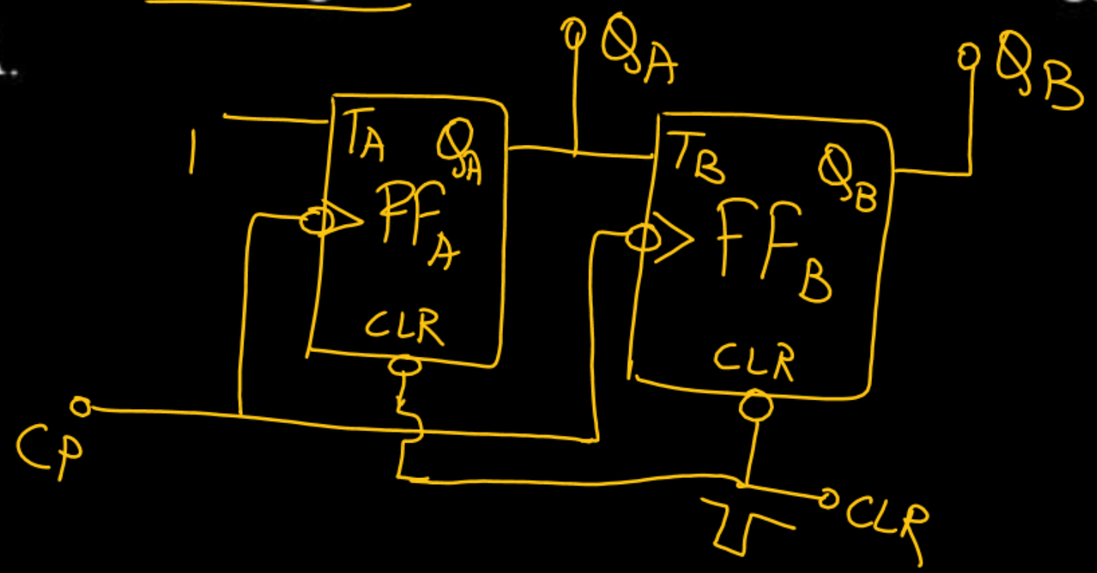
Waveforms



2 bit Synchronous counters

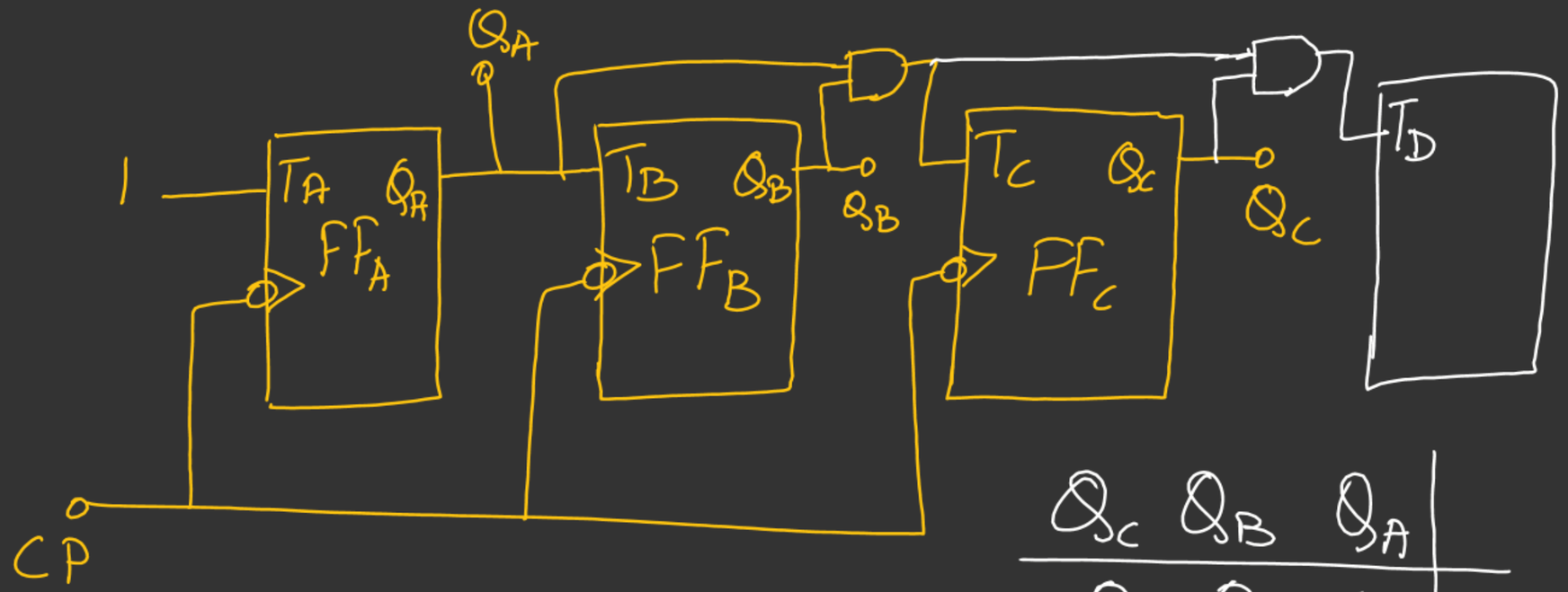
- If the "clock" pulses are applied to all the flip-flops in a counter simultaneously, then such a counter is called as synchronous counter.
- 2-bit Synchronous up counter
- The JA and KA inputs of FF-A are tied to logic 1. So FF-A will work as a toggle flip-flop. The JB and KB inputs are connected to QA.

CLR	Q_B	Q_A	Dcc
Initial	0	0	0
↓	0	1	1
↓	1	0	2
↓	1	1	3
↓	0	0	0



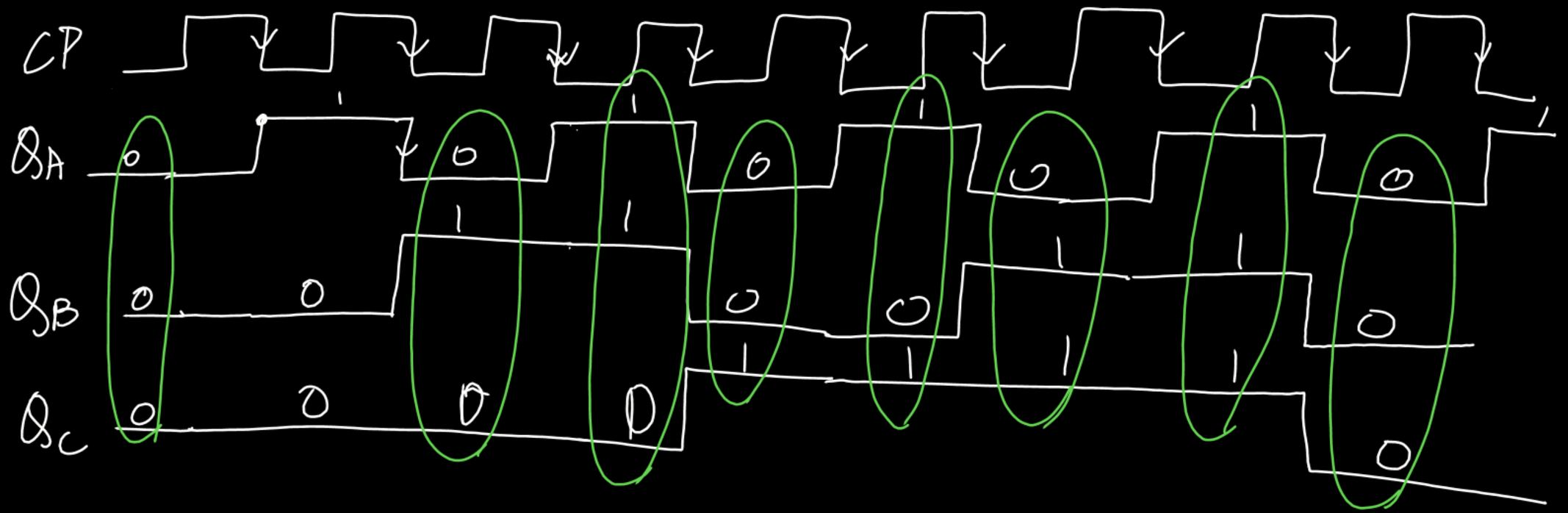
3 bit Synchronous Binary Up Counter

- Contains three T flip-flops & one 2-input AND gate.
- All flip-flops are negative edge triggered
- outputs of flip-flops change synchronously
- T inputs of first, second and third flip-flops are 1
- The output of first T flip-flop toggles for every negative edge of clock signal
- The output of second T flip-flop toggles for every negative edge of clock signal if Q0=1
- The output of third T flip-flop toggles for every negative edge of clock signal if both Q0 & Q1 are 1.



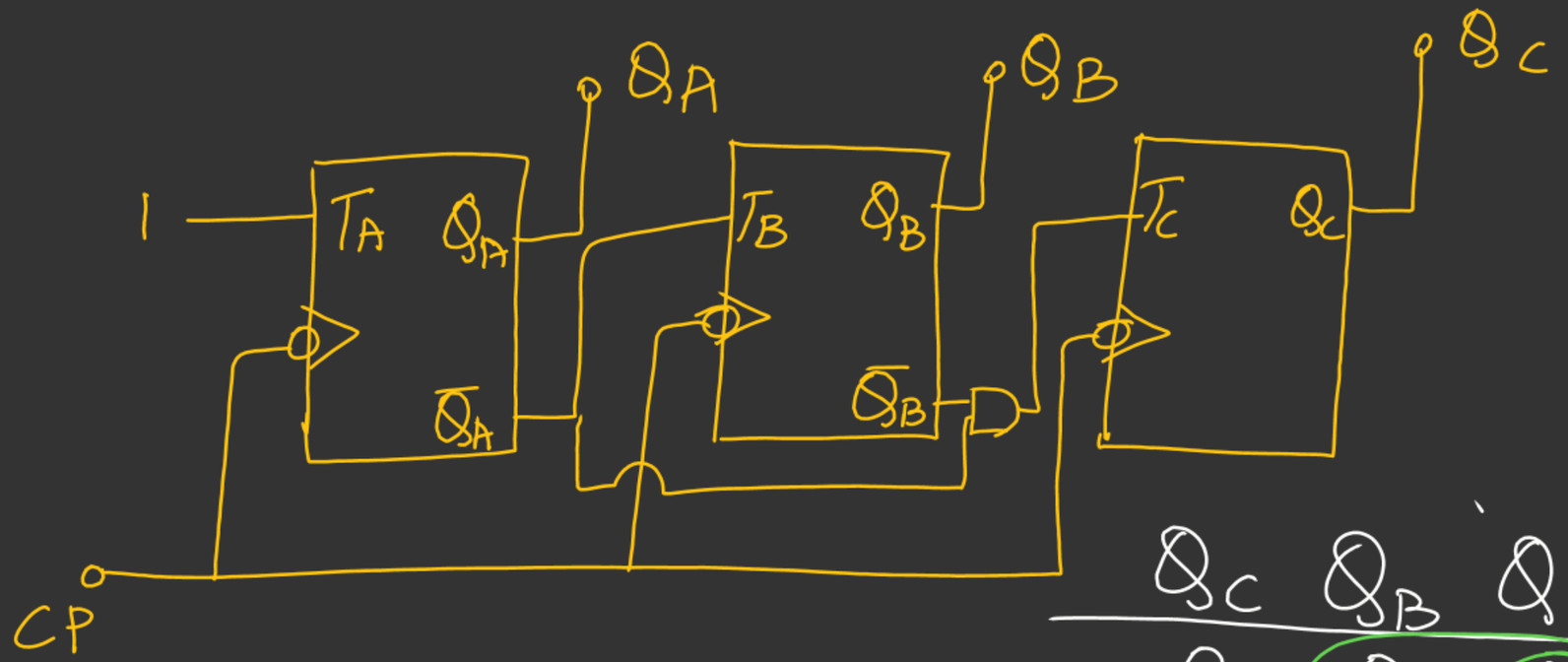
Q_C	Q_B	Q_A
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

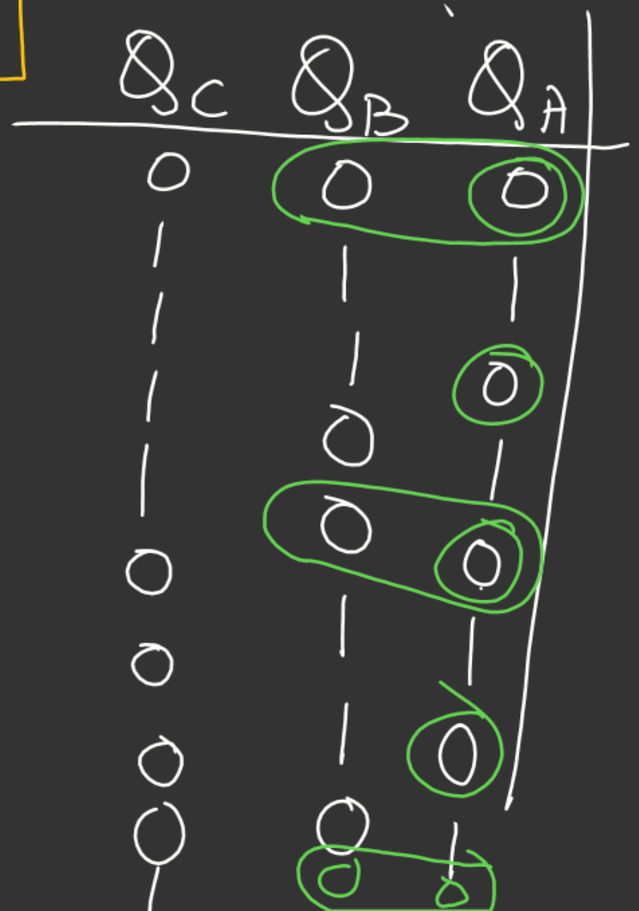
Waveforms



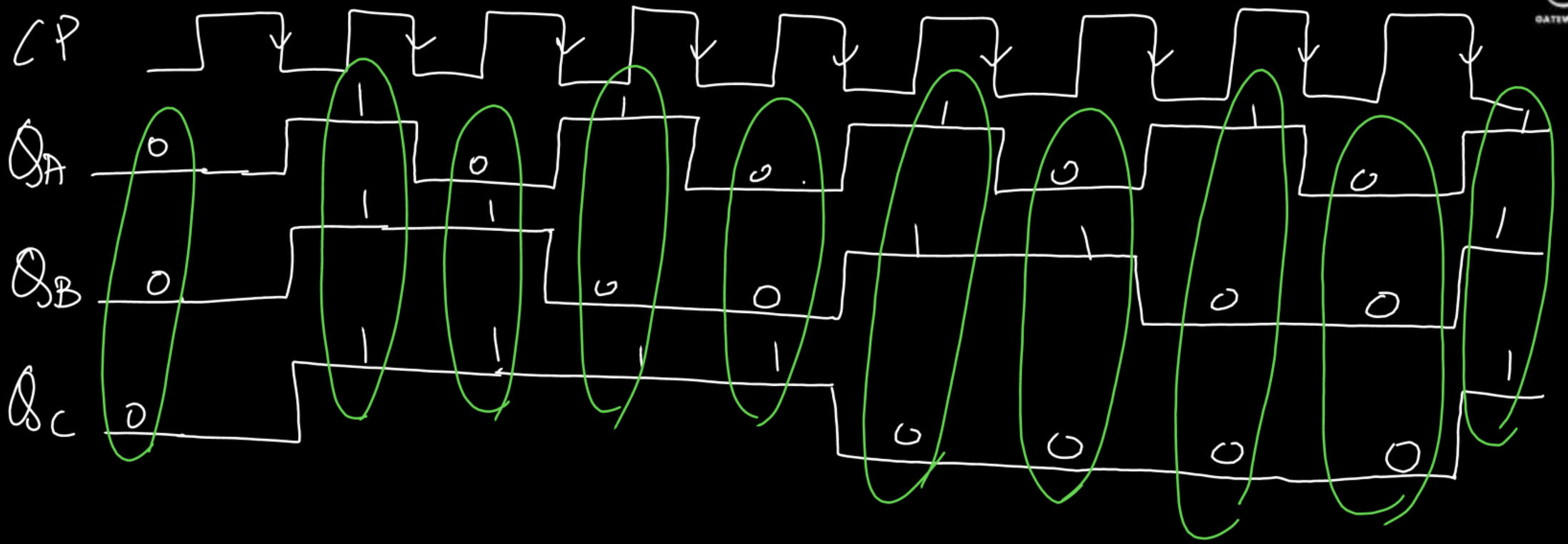
3 bit Synchronous Binary Down Counter

- contains three T flip-flops & one 2-input AND gate
- All these flip-flops are negative edge triggered
- outputs of flip-flops change synchronously.
- T inputs of first, second and third flip-flops are 1
- The output of first T flip-flop **toggles** for every negative edge of clock signal.
- The output of second T flip-flop toggles for every negative edge of clock signal if Q0′=1.
- The output of third T flip-flop toggles for every negative edge of clock signal if both Q1′ & Q0′ are 1.


1
T_A
Q_A
$\overline{Q}_A$
T_B
Q_B
$\overline{Q}_B$
T_C
Q_C
CP


Q_C
Q_B
Q_A

Waveforms



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