AKTU

GATEWAY CLASSES

Digital System Design

B.Tech. 3rd Sem

EC & Allied



Exam/Result Oriented Content

- ✓ Recorded Video Lectures
- ✓ Pdf Notes
- ✓ PYQs

DIGITAL SYSTEM DESIGN

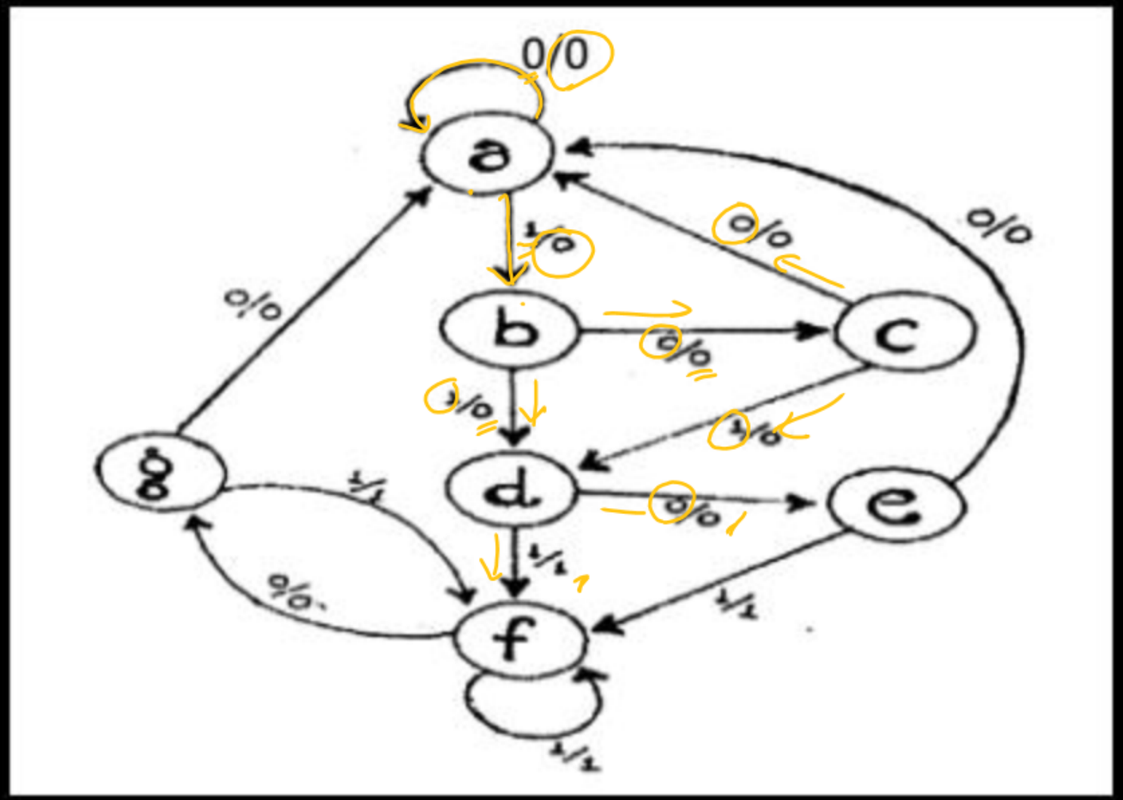
UNIT 3 : Sequential logic design

Lec 10

Today's Target

- State Reduction ✓
- Numerical Practice ✓

Draw the reduced state' table and reduced state diagram for ;the siate table given below:



State Table

P. S.	N. S. x=0	N. S. x=1	O/P x=0	O/P x=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

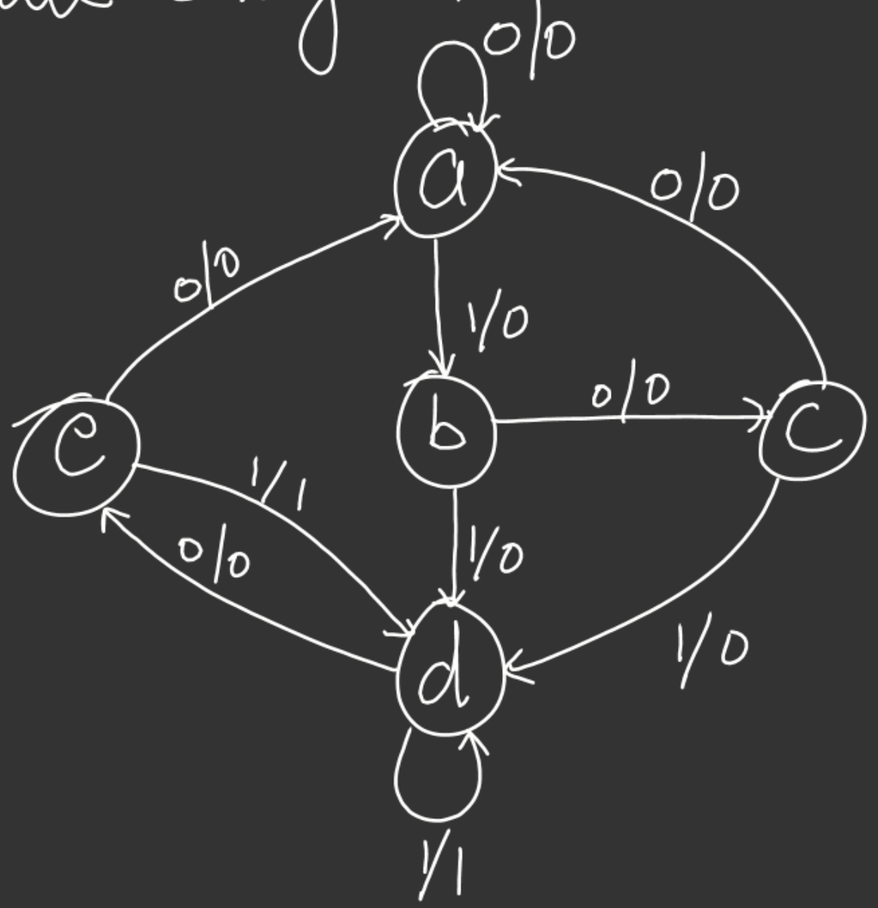
Reduced State Table

P.S.	N.S. $x=0$	N.S. $x=1$	O/P $x=0$	O/P $x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	~~g~~e	f	0	1

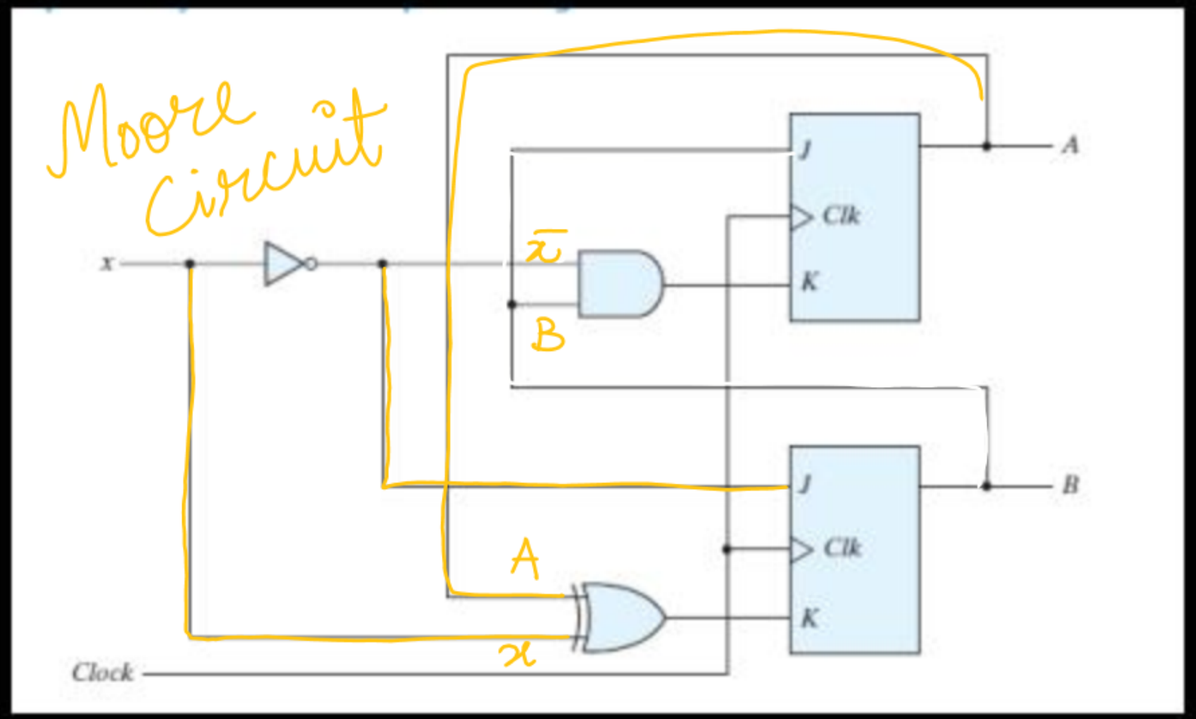
Reduced State Table

P.S.	N.S. $x=0$	N.S. $x=1$	O/P $x=0$	O/P $x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	~~f~~d	0	1
e	a	~~f~~d	0	1

State Diagram



Derive the State Table, State equations and State Diagram for the given circuit:



State Equations:

$J_A = B$

$K_A = B\bar{x}$

$J_B = \bar{x}$

$K_B = A \oplus x$

State Table

P.S			N.S					
A	B	x	A_{n+1}	B_{n+1}	J_A	K_A	J_B	K_B

State Eq^n

$J_A = B$

$K_A = B\bar{x}$

$J_B = \bar{x}$

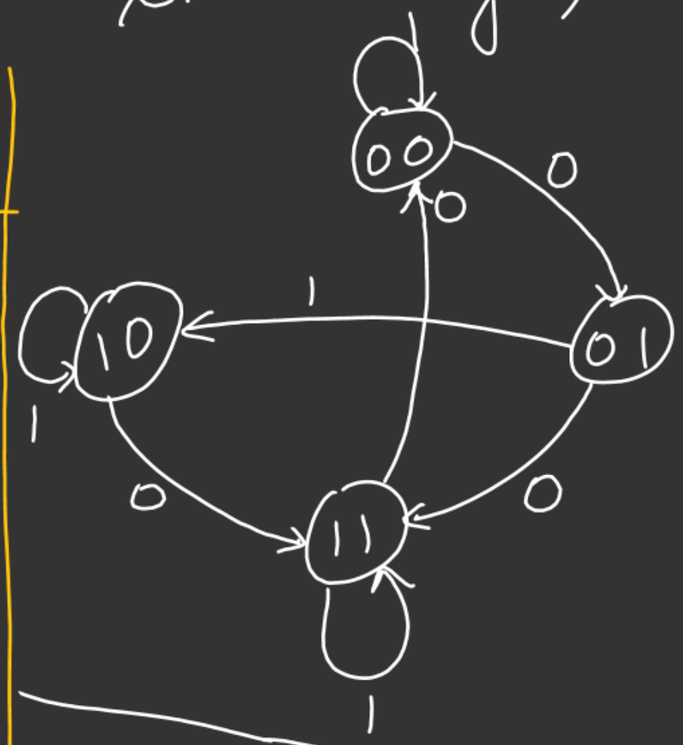
$K_B = A \oplus x$

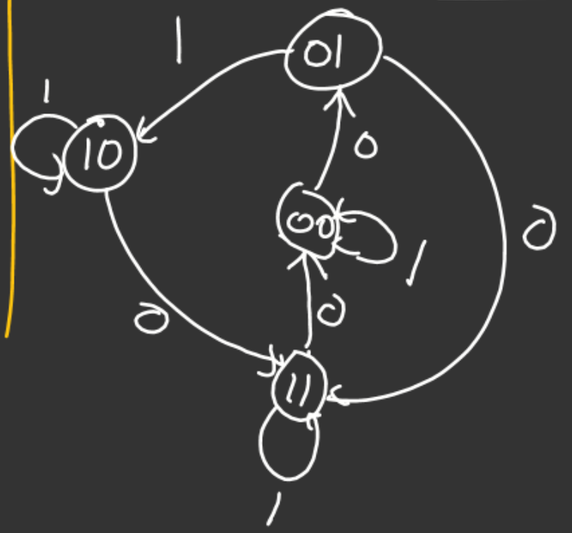
J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

State Table

P.S A	P.S B	i/p x	N.S. A_{n+1}	N.S. B_{n+1}	FF i/Ps J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

State Diagram





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Link in Description

Thank You