AKTU

GATEWAY CLASSES

Digital System Design

B.Tech. 3rd Sem

EC & Allied



Exam/Result Oriented Content

- ✓ Recorded Video Lectures
- ✓ Pdf Notes
- ✓ PYQs

DIGITAL SYSTEM DESIGN

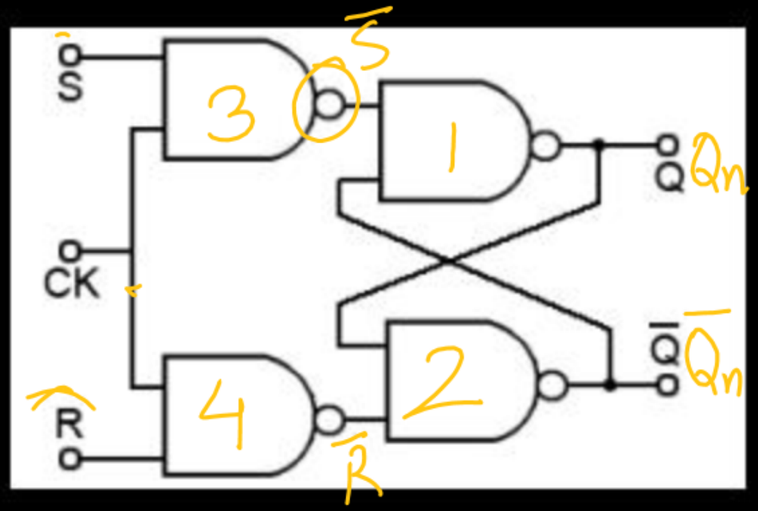
UNIT 3 : Sequential logic design

Lec 2

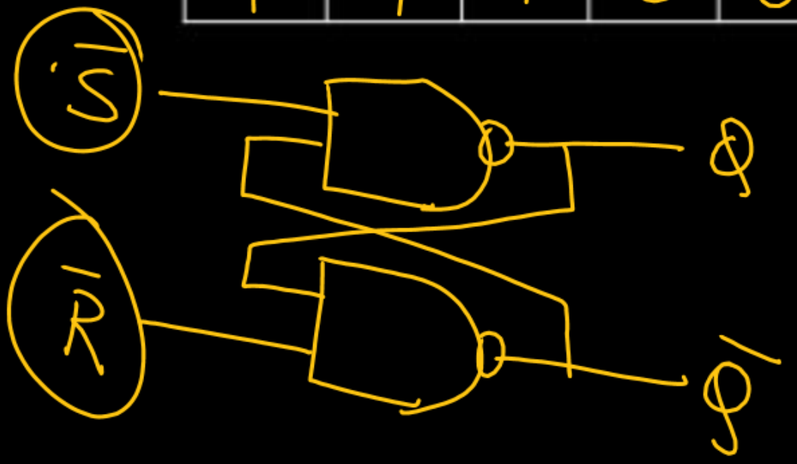
Today's Target

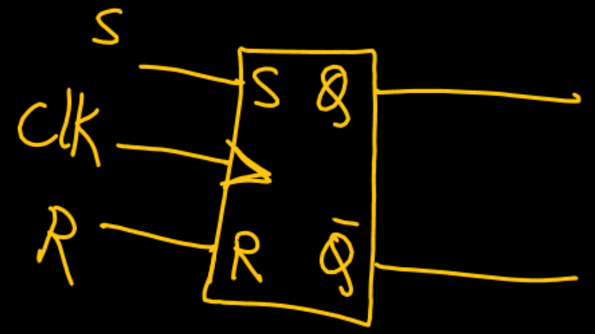
- CLOCKED FLIP FLOP
- D Flip Flop
- J-K Flip Flop
- T Flip Flop
- Race around condition in JK flip-flop
- Master-Slave Flip Flop
- UNIVERSITY QUESTIONS

CLOCKED FLIP FLOP



Input					Output		Status of Output
CLK	S	R	S'	R'	Qn+1	Qn+1'	
0	X	X	X	X	Qn	$\overline{Qn}$	No change
1	0	0	1	1	Qn	$\overline{Qn}$	Mem
1	0	1	1	0	0	1	Reset
1	1	0	0	1	1	0	Set
1	1	1	0	0	1	1	Invalid

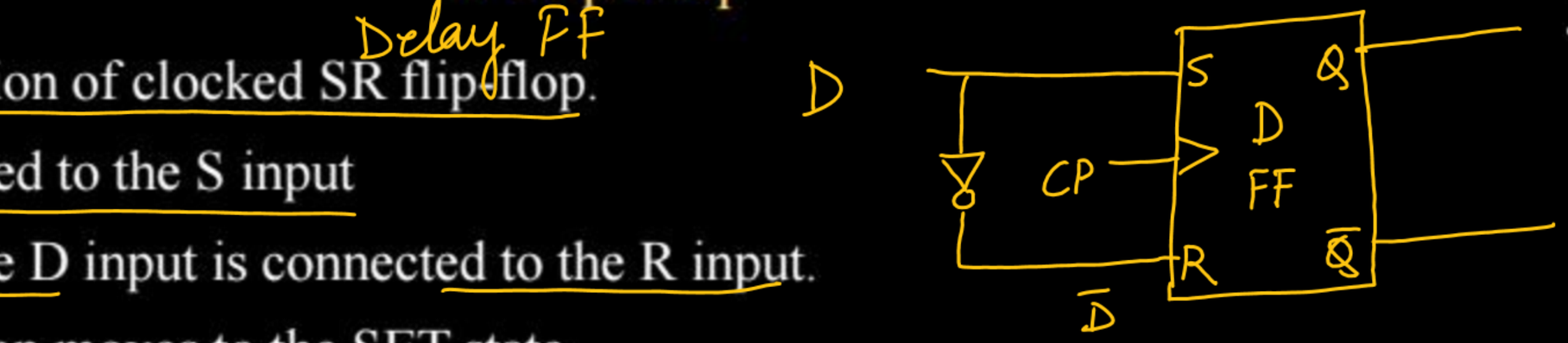


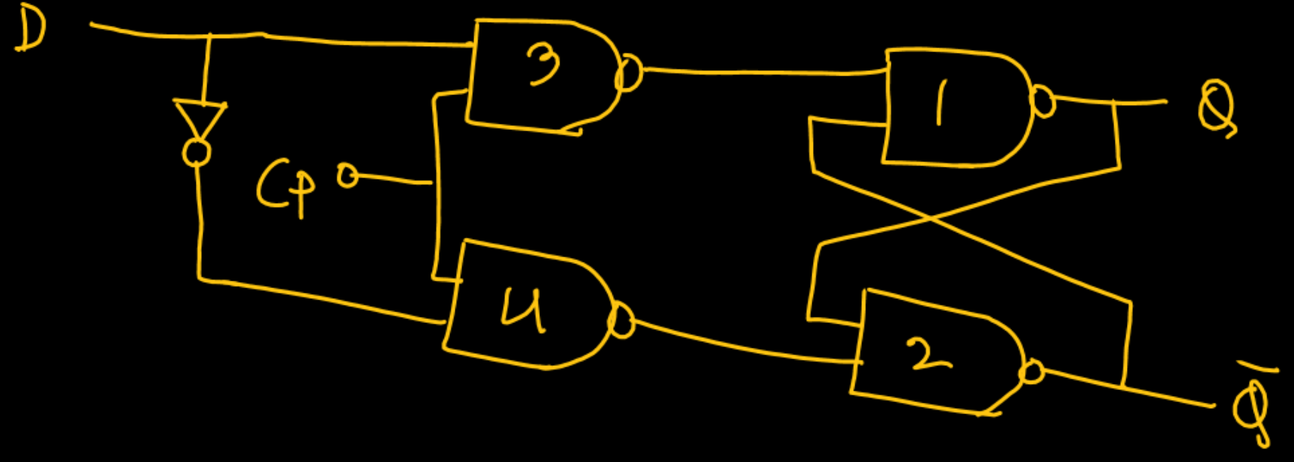


D Flip Flop

Delay FF

- a slight modification of clocked SR flip flop.
- D input is connected to the S input
- complement of the D input is connected to the R input.
- When D=1; flip flop moves to the SET state
- When D=0; flip flop switches to the CLEAR state.

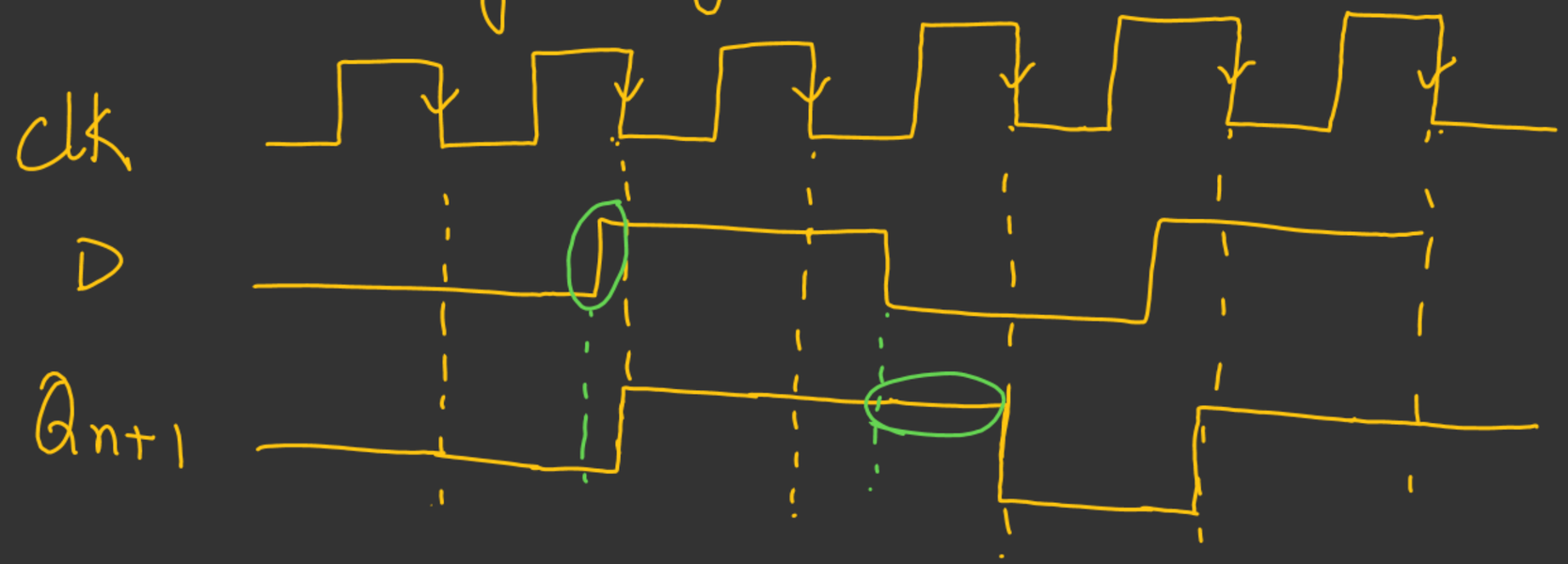




Truth Table

CP	D	Qn+1	
0	X	Qn	No change
1	0	0	Reset/Clear
1	1	1	Set

Timing Diagram

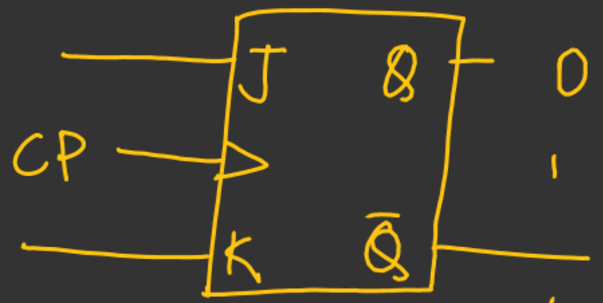


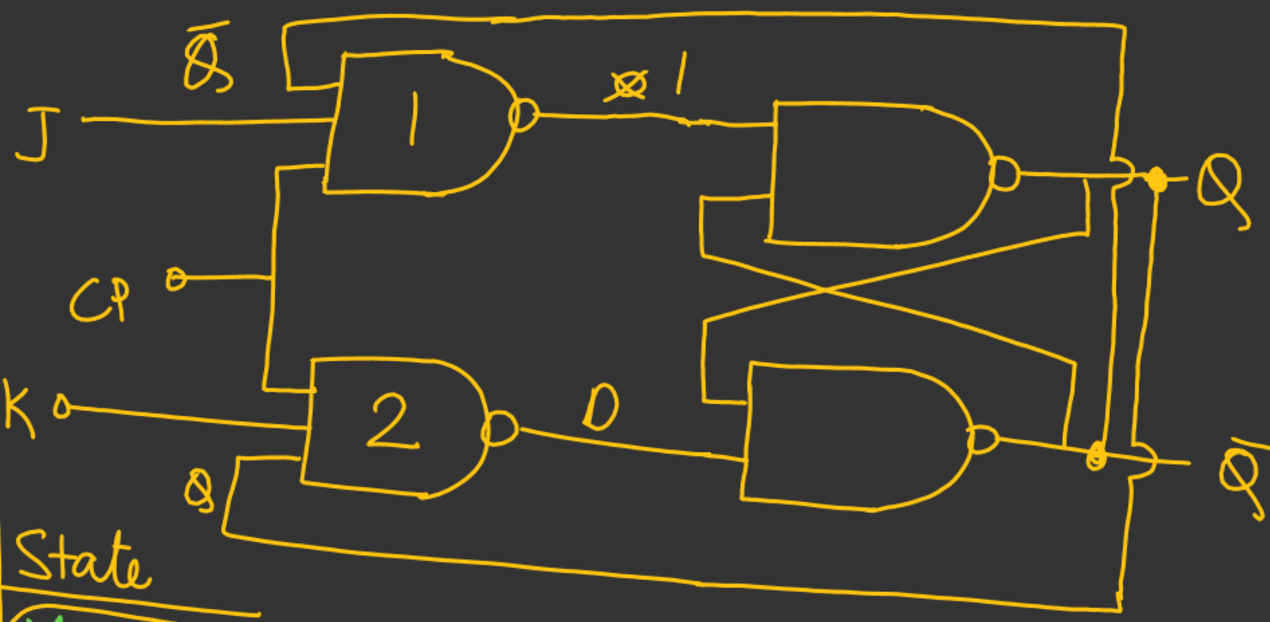
PROBLEM IN SR FF

- WHEN S=1: Q=1 (SET STATE)
- WHEN S=0: Q=0 (RESET/CLEAR STATE)
- WHEN S=R=0: Q= PREVIOUS STATE (MEMORY)
- WHEN S=R=1: Q= Q'= 1(INVALID CONDITION)
- To overcome this invalid/ undefined condition, we need to add some more gates.

S	R	Q_{n+1}
0	0	Mem
0	1	0
1	0	1
1	1	Invalid

JK-FF





0 → 1

1 → 1 → 0

1 → 0

0 → 1

Truth Table

J	K	Q_{n+1}	$\bar{Q}_{n+1}$	State
0	0	Q_n	$\bar{Q}_n$	Memory
0	1	0	1	Reset
1	0	1	0	Set
1	1	$\bar{Q}_n$	Q_n	Complement of Previous o/p

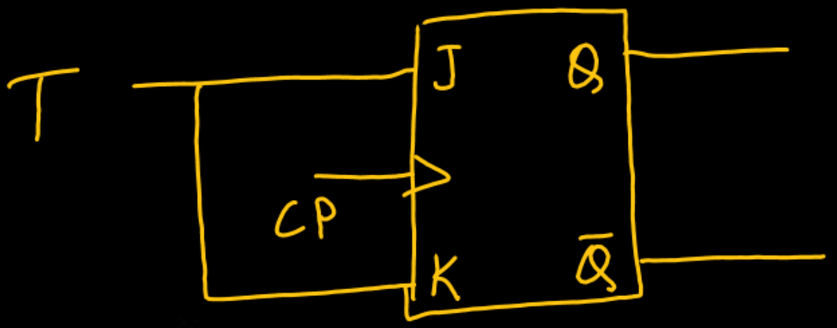
J-K Flip Flop

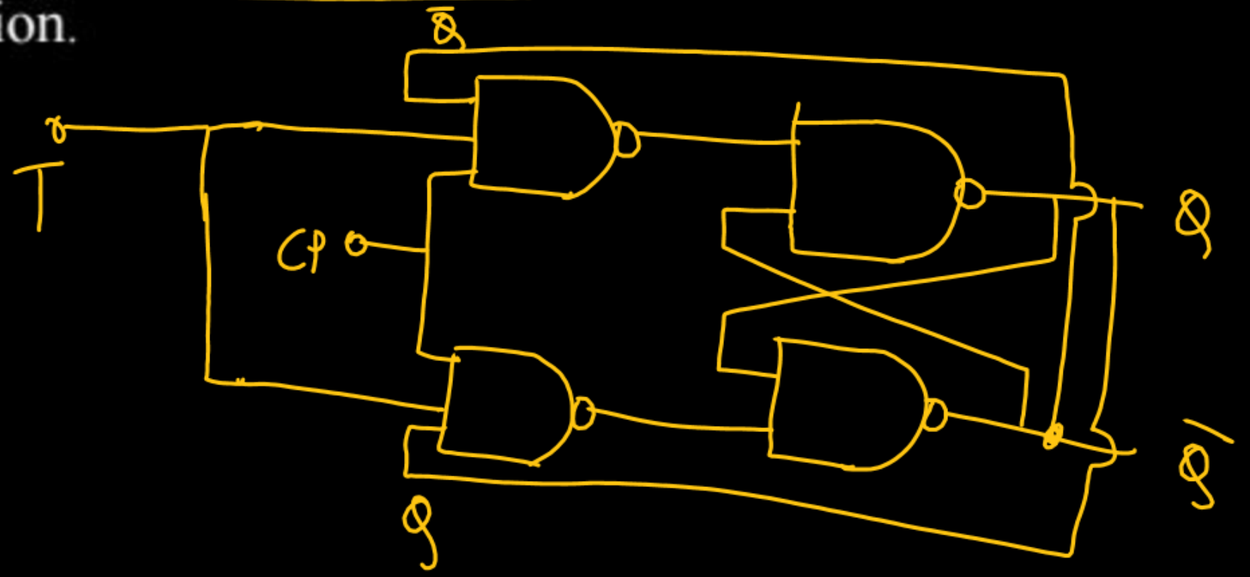
Jack & keying FF

- Also defined as a modification of the S-R flip flop.
- intermediate state is more refined and precise than that of a S-R flip flop.
- J (Jack) resembles S for SET and K(Keying) resembles R for RESET.
- When J=K=1; the flip-flop switch to the complement state
- i.e. for Q = 1, it switches to Q=0 and
  for Q = 0, it switches to Q=1.

T Flip Flop

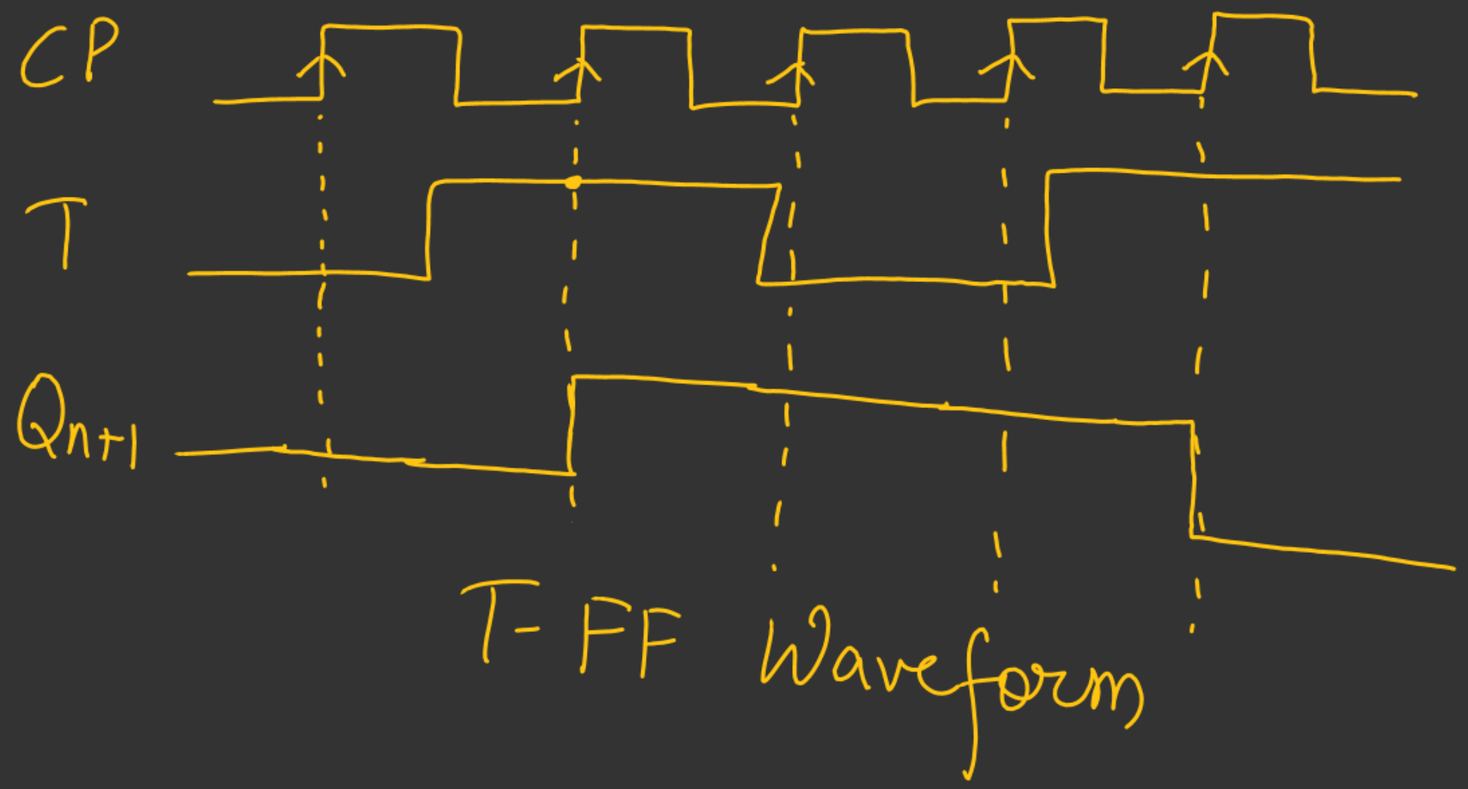
- much simpler version of the J-K flip flop
- Both the J and K inputs are connected together
- also called a single input J-K flip flop
- When clock pulse is given to the flip flop, the output begins to toggle
- the restriction on the pulse width can be eliminated with a master-slave or edge-triggered construction.





Truth Table

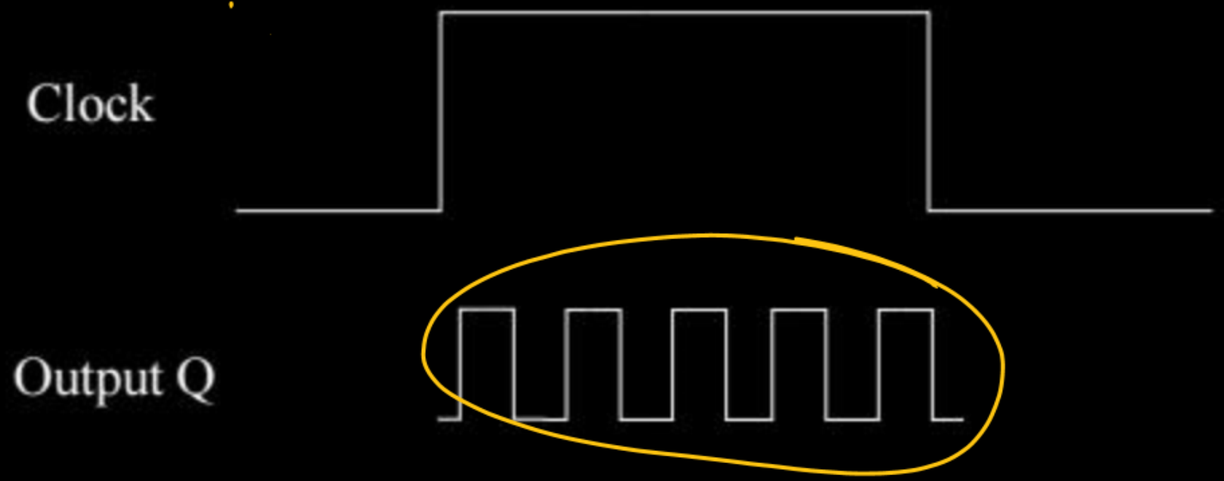
CP	T	Q_{n+1}
0	X	Q_n
1	0	Q_n (Mem)
1	1	$\bar{Q}_n$ (Toggle o/p)



T- FF Waveform

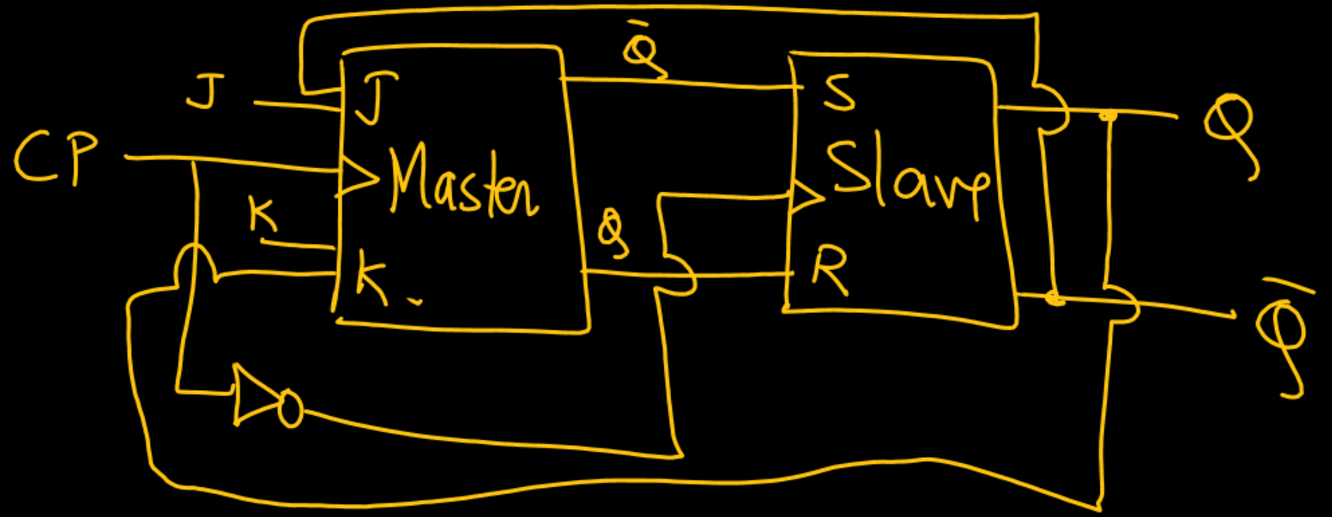
Race around condition in JK flip-flop:

- In JK flip flop as long as clock is high for the input conditions J=K=1
- the output changes or complements its output from 1–>0 and 0–>1.
- This is called toggling output or uncontrolled changing or racing condition.



Steps to avoid racing condition in JK Flip flop:

- If the Clock On or High time is less than the propagation delay of the flip flop then racing can be avoided.
- This is done by using edge triggering rather than level triggering.
- If the flip flop is made to toggle over one clock period then racing can be avoided.
- This introduced the concept of Master Slave JK flip flop.

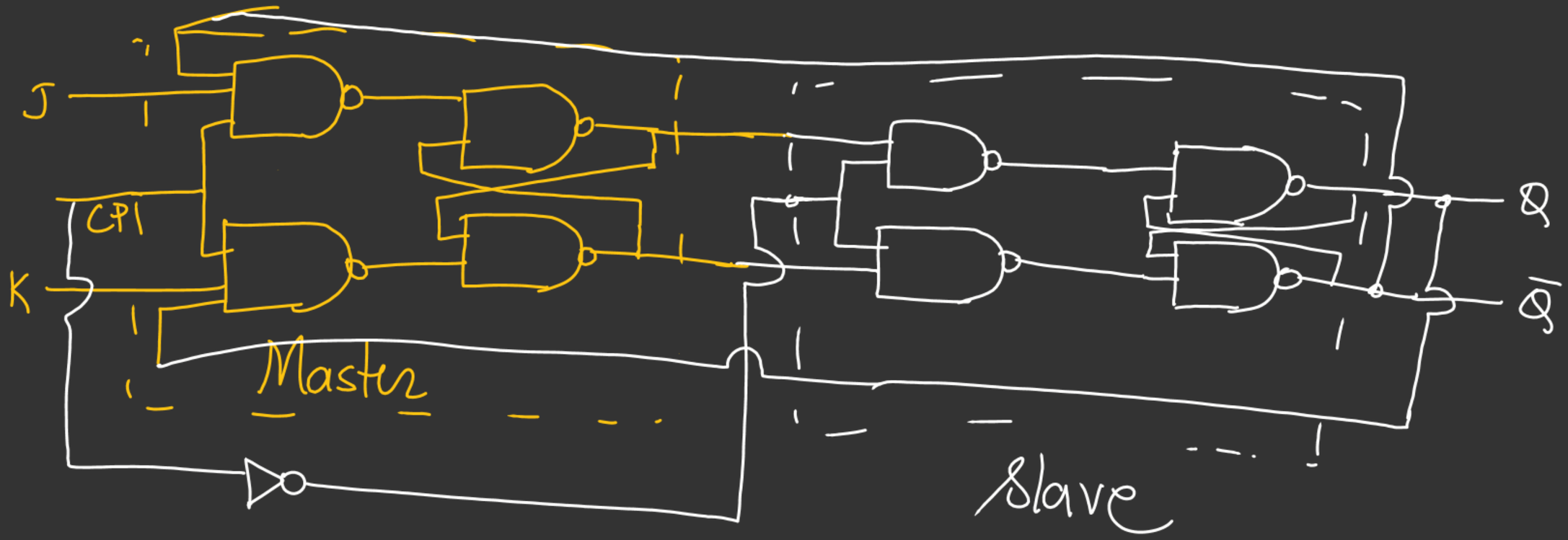


Master-Slave Flip Flop

- Master-slave flip flop is designed using two separate flip flops.
- Out of these, one acts as the master and the other as a slave.
- both the J-K flip flops are presented in a series connection.
- The output of the master J-K flip flop is fed to the input of the slave J-K flip flop.
- The output of the slave J-K flip flop is given as a feedback to the input of the master J-K flip flop.
- The clock pulse [Clk] is given to the master J-K flip flop and it is sent inverted to the slave J-K flip flop.

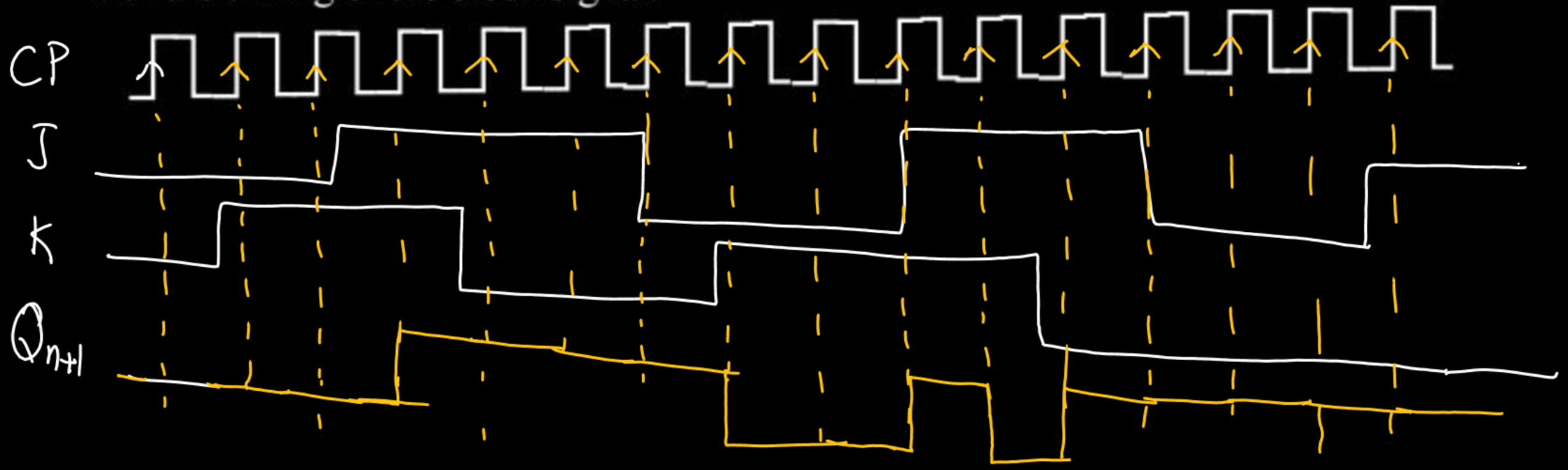
Working of M-S FF

- When Clk=1, the master J-K flip flop gets disabled. enabled
- The Clk input of the master input will be the opposite of the slave input.
- So the master flip flop output will be recognized by the slave flip flop only when the Clk value becomes 0.
- when the clock pulse males a transition from 1 to 0, the locked outputs of the master flip flop are fed through to the inputs of the slave flip-flop making this flip flop edge or pulse-triggered.


J
CP1
K
Master
Slave
Q
$\bar{Q}$

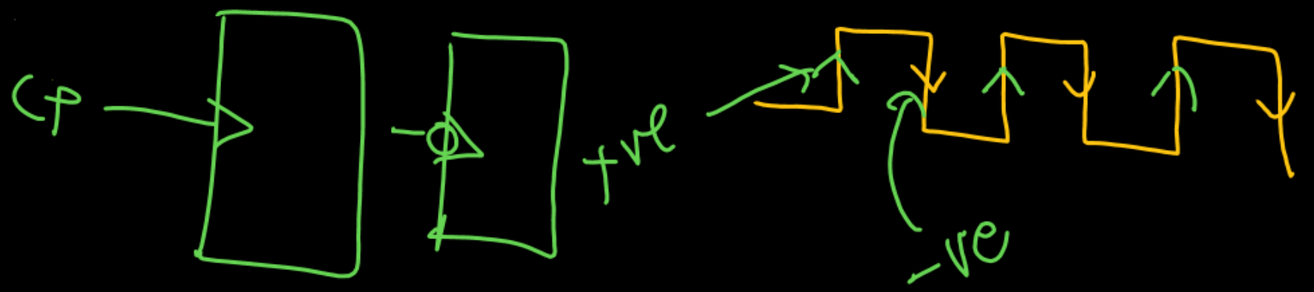
TIMING DIAGRAM

- The circuit accepts the value in the input when the clock is HIGH, and passes the data to the output on the falling-edge of the clock signal.
- This makes the Master-Slave J-K flip flop a Synchronous device as it only passes data with the timing of the clock signal.



UNIVERSITY QUESTIONS

YEAR	QUESTIONS	MARKS
22-23, 19-20	What do you mean by race around condition in JK Flip Flop?	2 Marks
21-22	Explain the working of Master-Slave JK flip-flop with the help of logic diagram, functional table, logic symbol.	10 Marks
21-22	Explain positive edge triggered D-flip-flop with the help of circuit diagram and waveforms.	10 Marks



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Thank You