AKTU

GATEWAY CLASSES

Digital System Design

B.Tech. 3rd Sem

EC & Allied



Exam/Result Oriented Content

- ✓ Recorded Video Lectures
- ✓ Pdf Notes
- ✓ PYQs

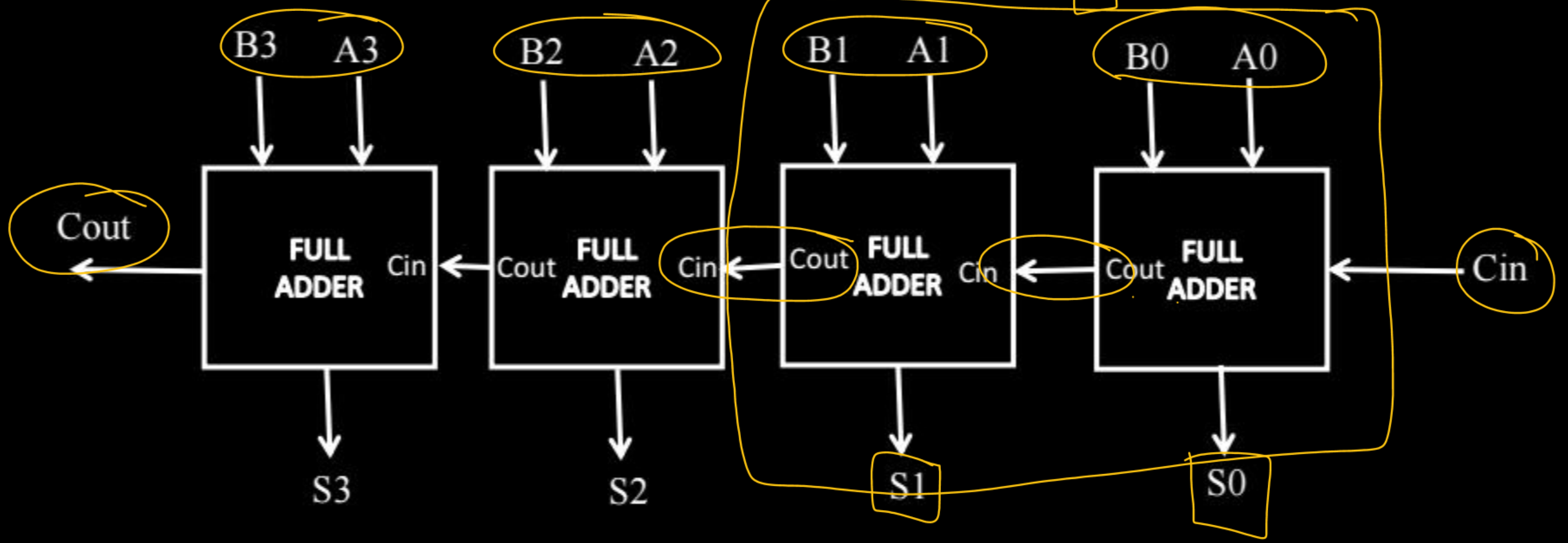
DIGITAL SYSTEM DESIGN

UNIT 2 : Combinational circuits

Today's Target

- A 4-bit Ripple Carry Adder
- Binary Subtractor
- Difference between Serial Adder and Parallel Adder
- Carry Look Ahead Adder
- DPP
- University Questions

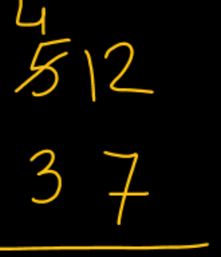
A 4-bit Ripple Carry Adder



Binary Subtractor

- produces an output which is the subtraction of two binary numbers.
- The binary subtractor produces a DIFFERENCE, D
- use a BORROW bit, B from the previous column.
- Binary subtraction Rules:
- 0 – 0 = 0
- 1 – 0 = 1
- 1 – 1 = 0
- 0 – 1 = 1, borrow = 1



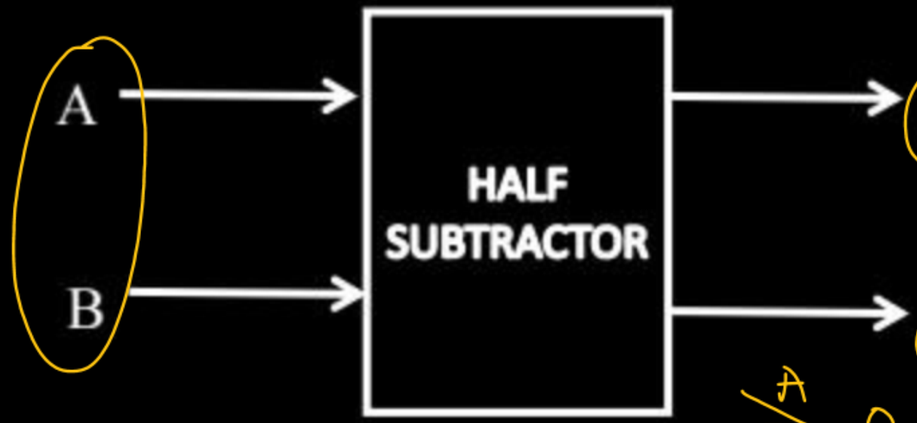




Bin

A Half Subtractor Circuit

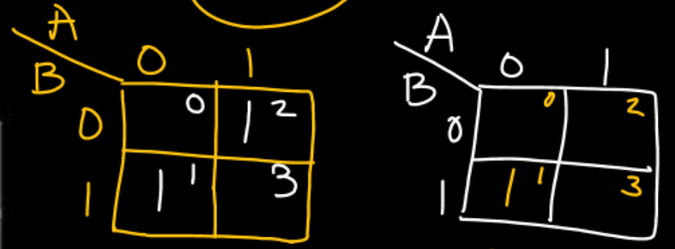
- A half subtractor is a logical circuit that performs a subtraction operation on two binary digits.
- The half subtractor produces a sum and a borrow bit for the next stage.



$D = \Sigma m(1, 2)$

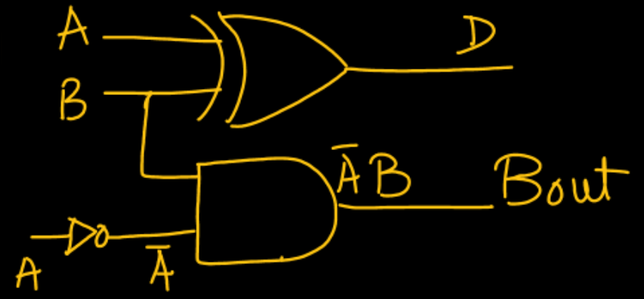
$Bout = \Sigma m(1)$

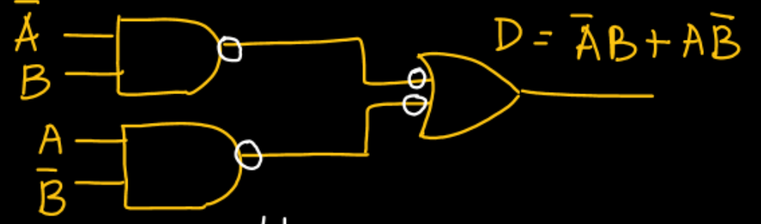
A	B	D	Bout
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

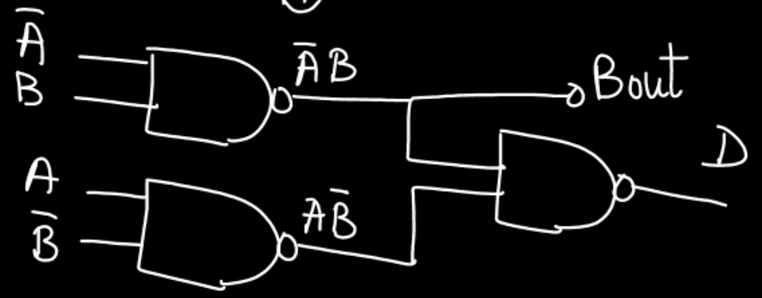


for $D = \bar{A}B + A\bar{B}$ ✓ for $B_{out} = \bar{A}B$

$= A \oplus B$ ×







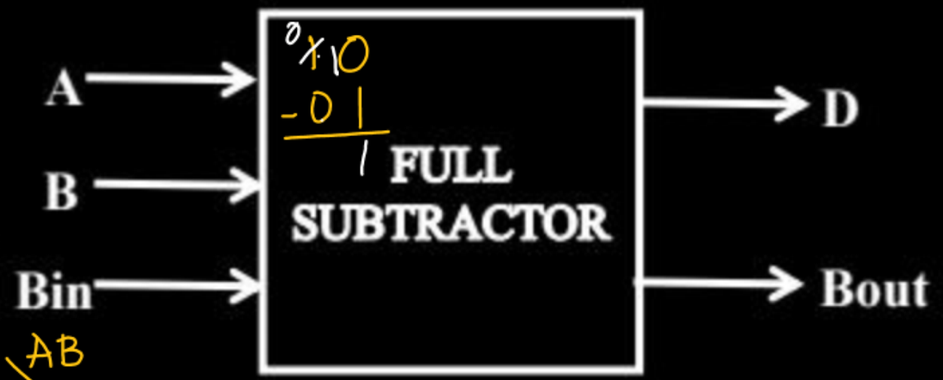
A Full Binary Subtractor Circuit

- a full subtractor has three inputs.
- The two single bit data inputs X (minuend) and Y (subtrahend)
- an additional *Borrow-in* (B-in) input to receive the borrow generated from a previous stage.

A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$D = \Sigma m(1,2,4,7)$

$Bout = \Sigma m(1,2,3,7)$



Bin \ AB	00	01	11	10
0	0	1	6	4
1	1	3	7	5

$$D = \bar{A}\bar{B}Bin + \bar{A}B\bar{Bin} + A\bar{B}\bar{Bin} + ABBin$$
$$= \bar{A}(\bar{B}Bin + B\bar{Bin}) + A(\bar{B}\bar{Bin} + BBin)$$
$$= \bar{A}(B \oplus Bin) + A\overline{(B \oplus Bin)}$$

If $B \oplus Bin = X$

$$D = \bar{A}X + A\bar{X}$$
$$= A \oplus X$$

$$\boxed{D = A \oplus B \oplus Bin}$$

K-Map for Bout

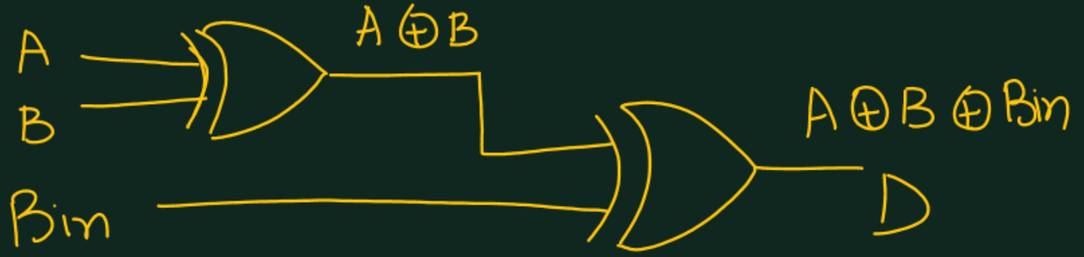
Bin \ AB	00	01	11	10
0	0	1	6	4
1	1	3	7	5

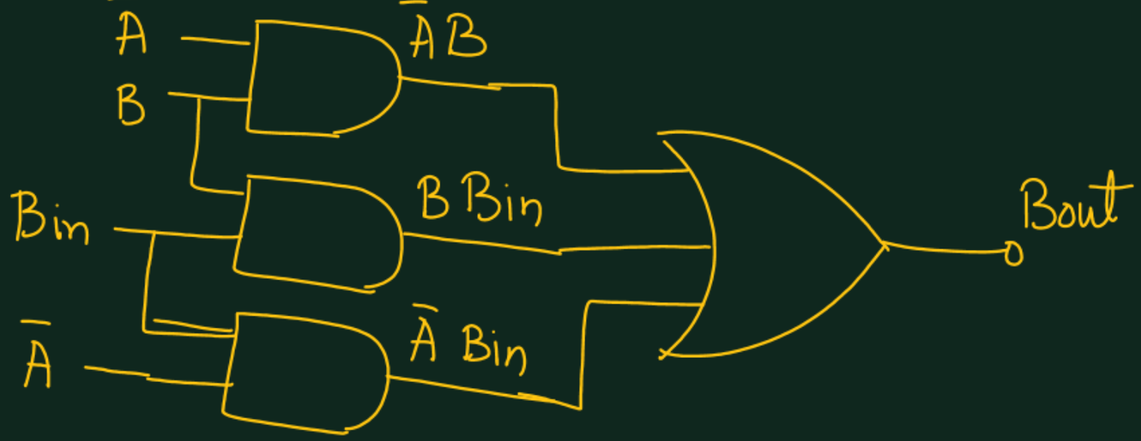
$$\boxed{Bout = \bar{A}Bin + \bar{A}B + BBin}$$

Using Logic Gates

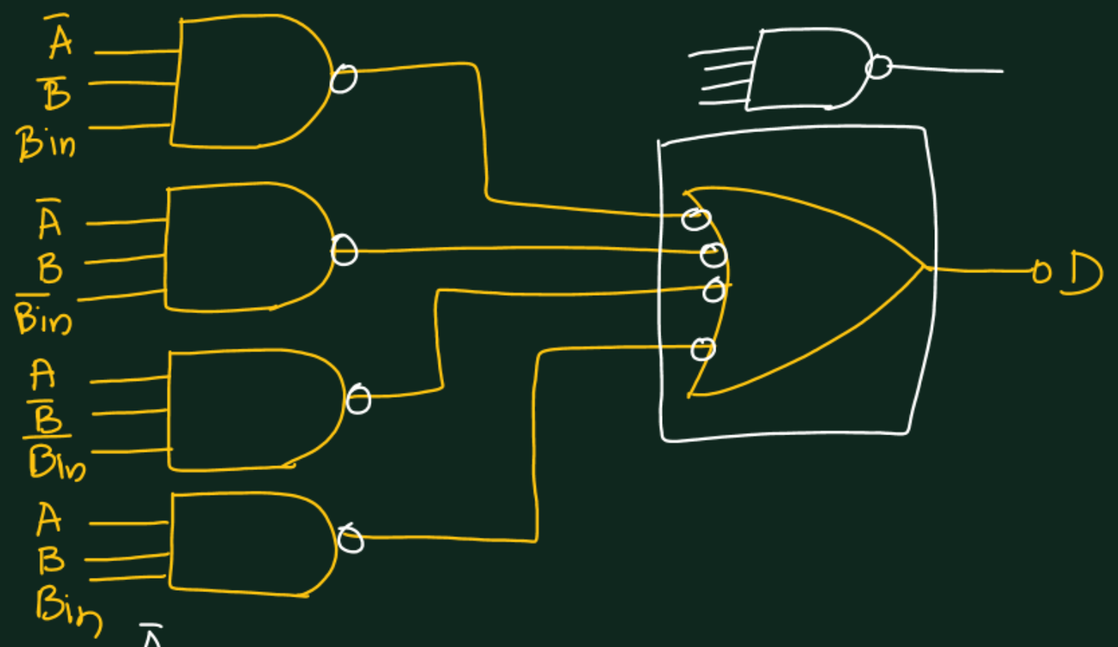
$D = A \oplus B \oplus Bin$

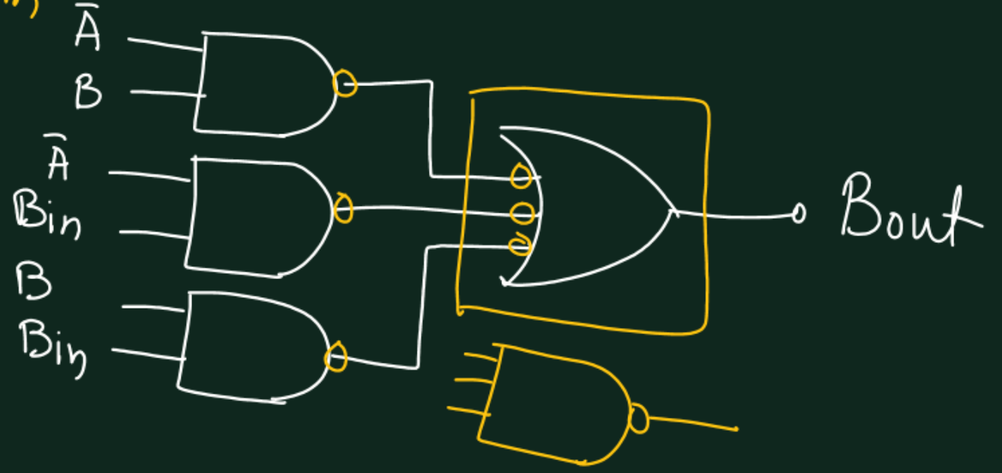
$Bout = \bar{A}B + \bar{A}Bin + BBin$





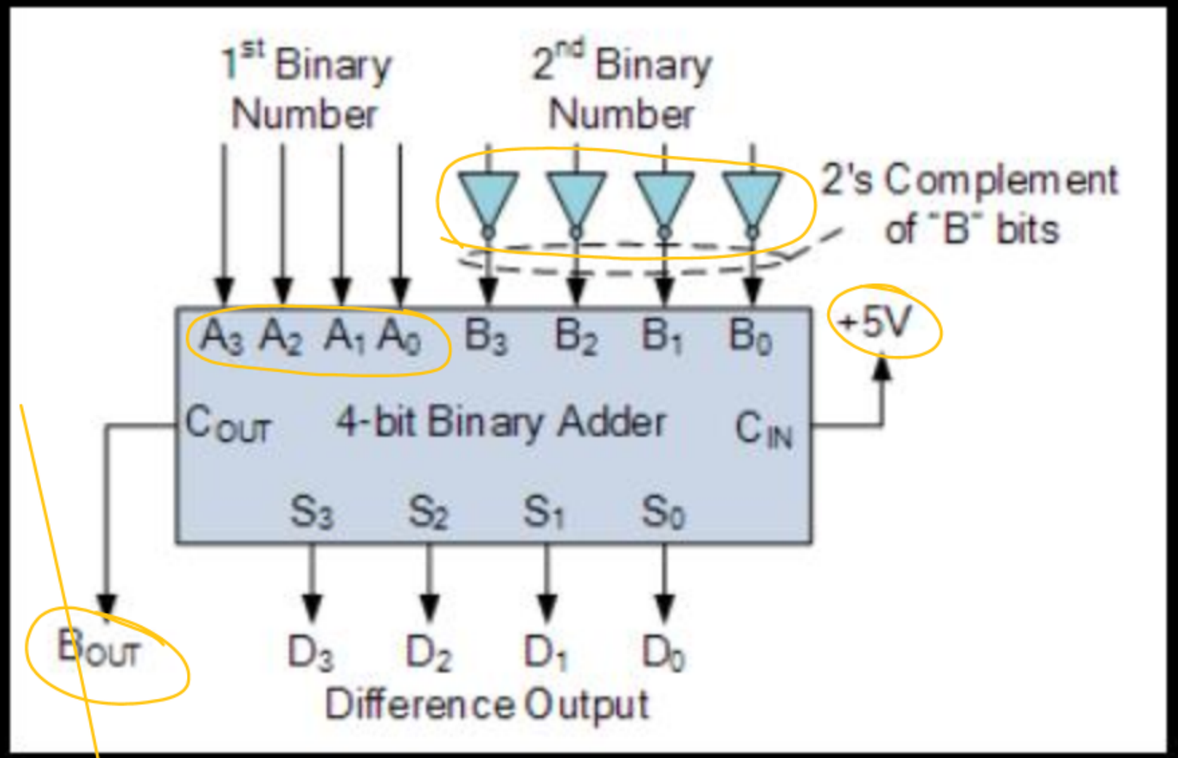
$D = \bar{A}\bar{B}Bin + \bar{A}B\bar{Bin} + A\bar{B}\bar{Bin} + ABBin$





An n-bit Binary Subtractor

- It uses an n-bit adder and n number of inverters (NOT Gates)
- the process of subtraction becomes an addition as we can use two's complement notation on all the bits in the subtrahend and setting the carry input of the least significant bit to a logic "1" (HIGH).



1011
− 0101

I: 1011
2's of II: +1011

1's + 1 = 2's

1 0110

0101
1's 1010
+ 1
1011

Difference between Serial Adder and Parallel Adder:

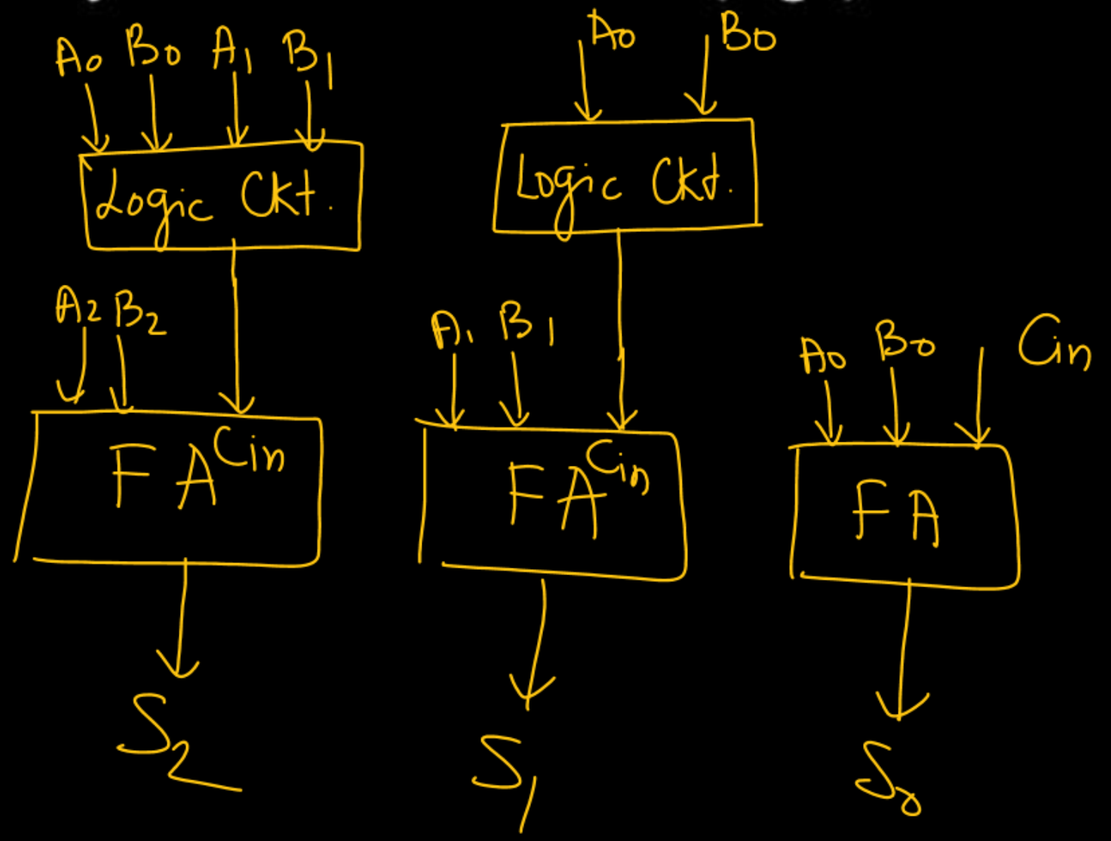
SERIAL ADDER	PARALLEL ADDER
It is used to add two binary numbers in serial form.	It is used to add two binary numbers in parallel form.
A serial adder uses shift registers.	A parallel adder uses registers with parallel loads.
It requires single full adder.	It requires multiple full adders
Carry flip-flop is used in serial adder.	Ripple carry adder is used in parallel adder.
Serial adder is a sequential circuit.	Parallel adder is a combinational circuit.
In serial adder, propagation delay is less.	In parallel adder, propagation delay is present from input carry to output carry.
Number of required full adder is fixed i.e. one.	Number of required full adder is equal to the number of bits in the binary number.

Difference between "Ripple Carry Adder" and Carry Look-ahead Generator

- In a ripple carry adder, the carry signal has to travel through each adder module to get to the end, causing long propagation delays.
- In a carry look-ahead adder, the carry logic is handled separately with shorter delays.
- A carry look-ahead adder reduces the propagation delay by introducing more complex hardware.

Carry Look Ahead Adder

- Carry Look Ahead Adder is an improved version of the ripple carry adder.
- It generates the carry-in of each full adder simultaneously without causing any delay.
- The time complexity of carry look ahead adder = Θ (logn).



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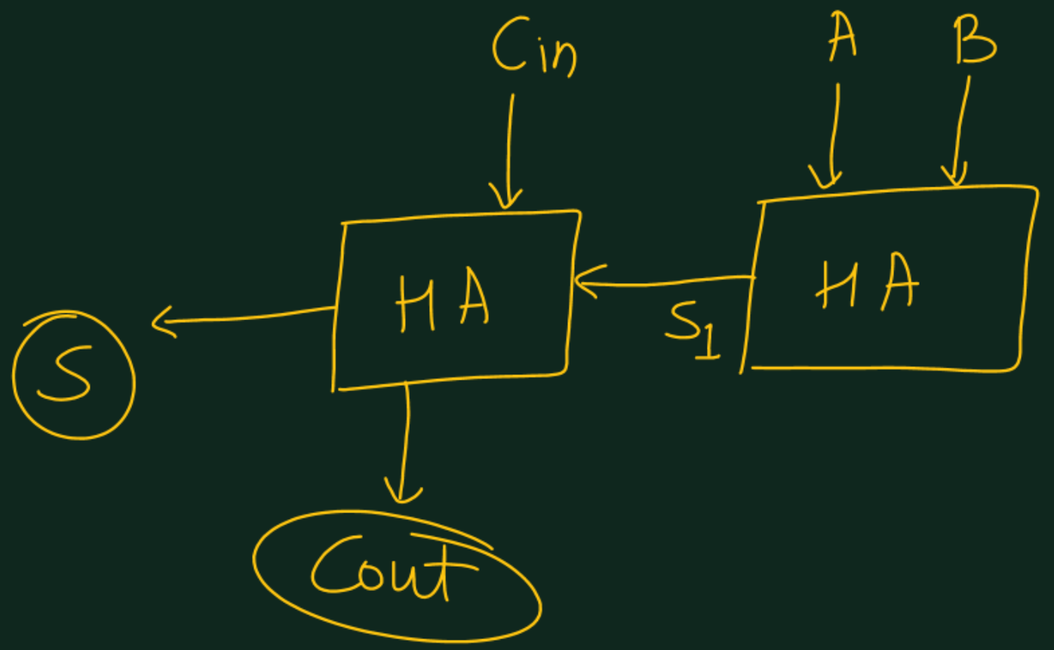
Implement using NAND gates only:

a) Half Subtractor ✓

b) Full Subtractor ✓

UNIVERSITY QUESTIONS

YEAR	QUESTION	MARKS
22-23	Draw a full adder using two half adders	2 marks
21-22	What is the role of subtractor in digital electronics?	2 marks
21-22	Construct half subtractor using NAND gates.	2 marks
21-22	Explain the concept of serial adder with accumulators.	10 marks
20-21	What is difference between “Ripple Carry Adder” and Carry Look-ahead Generator?	2 marks
19-20	Construct half subtractor using logic gates.	2 marks
19-20	Design a 4-bit parallel binary Adder/Subtractor circuit.	10 marks


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Thank You

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