AKTU

GATEWAY CLASSES

Digital System Design

B.Tech. 3rd Sem
EC & Allied

Exam/Result Oriented Content

- ✓ Recorded Video Lectures
- ✓ Pdf Notes
- ✓ PYQs



DIGITAL SYSTEM DESIGN

UNIT 3 : Sequential logic design

Lec-1

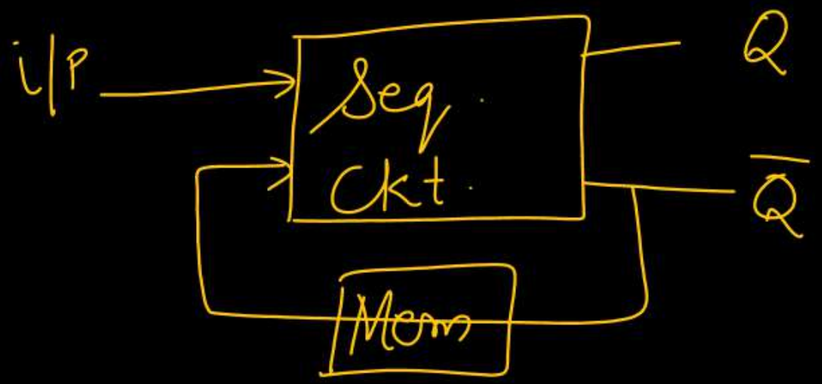
Today's Target

- Introduction of Sequential circuit
- Difference between combinational and sequential circuit
- Sequential Logic Representation
- Classification of Sequential Logic
- Latches and flip-flops
- University Questions

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Introduction of Sequential circuit

- Circuits whose output depends upon both the present input of the circuit and its previous state.
- We need circuits that have memory.
- Three characteristics are:
  - ➢ the device must have two stable states
  - ➢ there must be a way to read the state of the device
  - ➢ there must be a way to set the state at least once.



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Difference between combinational and sequential circuit

Sr. No.	Key	Combinational Circuit	Sequential Circuit
1	Definition	Combinational Circuit is the type of circuit in which output is independent of time and only relies on the input present at that particular instant.	On other hand Sequential circuit is the type of circuit where output not only relies on the current input but also depends on the previous output.
2	Feedback	In Combinational circuit as output does not depend on the time instant, no feedback is required for its next output generation.	On other hand in case of Sequential circuit output relies on its previous feedback so output of previous input is being transferred as feedback used with input for next output generation.
3	Performance	As the input of current instant is only required in case of Combinational circuit, it is faster and better in performance as compared to that of Sequential circuit.	On other hand Sequential circuit are comparatively slower and has low performance as compared to that of Combinational circuit.

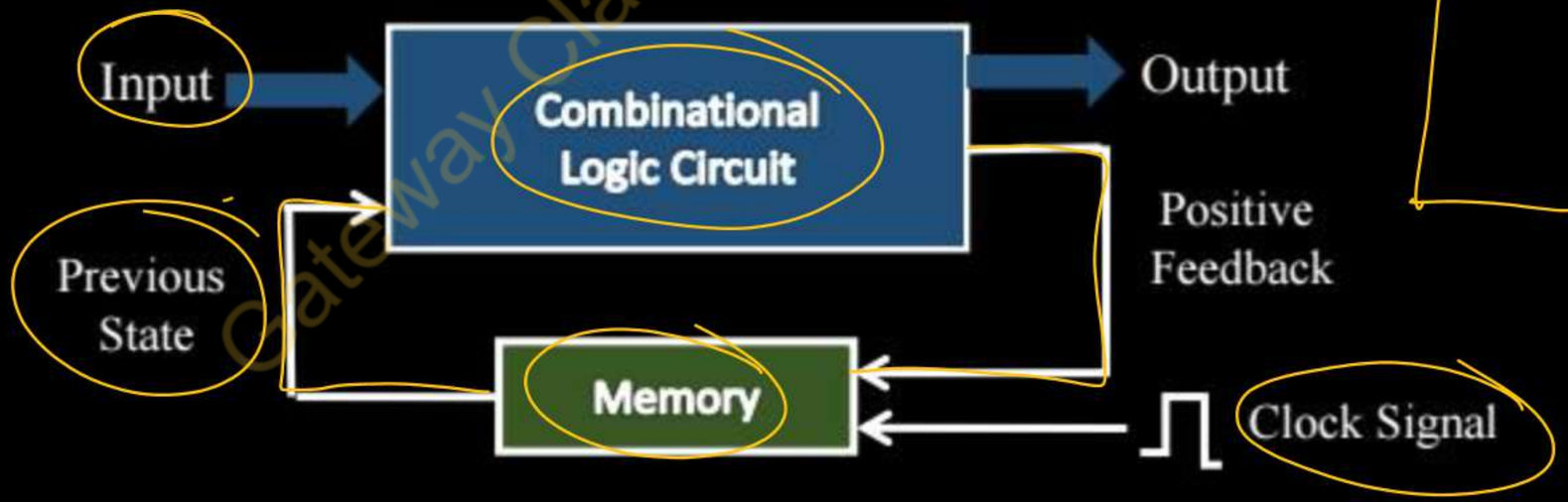
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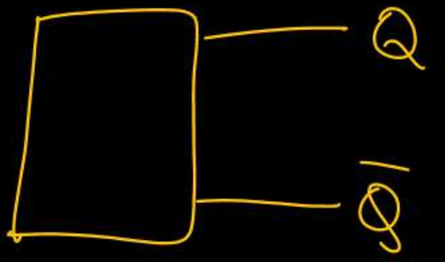
Sr. No.	Key	Combinational Circuit	Sequential Circuit
4	Complexity	No implementation of feedback makes the combinational circuit less complex as compared to sequential circuit.	However on other hand implementation of feedback makes sequential circuit more complex as compared to combinational circuit.
5	Elementary Blocks	Elementary building blocks for combinational circuit are logic gates.	On other hand building blocks for sequential circuit are flip flops..
6	Operation	Combinational circuit are mainly used for arithmetic as well as Boolean operations.	On other hand Sequential circuit is mainly used for storing data.

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Sequential Logic Representation

- The word "Sequential" means that things happen in a "sequence", one after another.
- The actual clock signal determines when things will happen next.
- Simple sequential logic circuits can be constructed from standard Bistable circuits such as: Flip-flops, Latches and Counters.
- Bistable circuits can be made by universal NAND Gates and/or NOR Gates in a particular combinational way.





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Classification of Sequential Logic

1. Event Driven – asynchronous circuits that change state immediately when enabled.

2. Clock Driven – synchronous circuits that are synchronised to a specific clock signal.

3. Pulse Driven – which is a combination of the two that responds to triggering pulses.

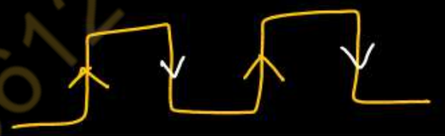


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Latches and flip-flops

- latches and flip-flops are the building blocks of sequential circuits.
- The difference between a latch and a flip-flop are:

E = 1

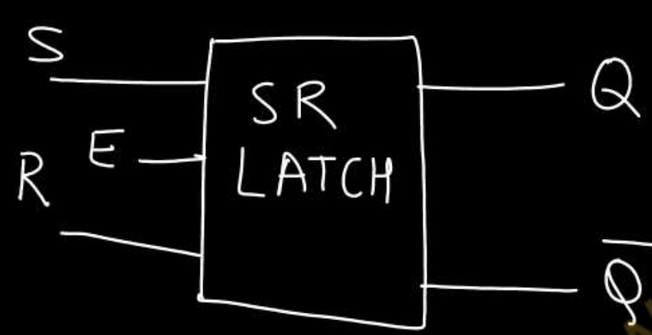


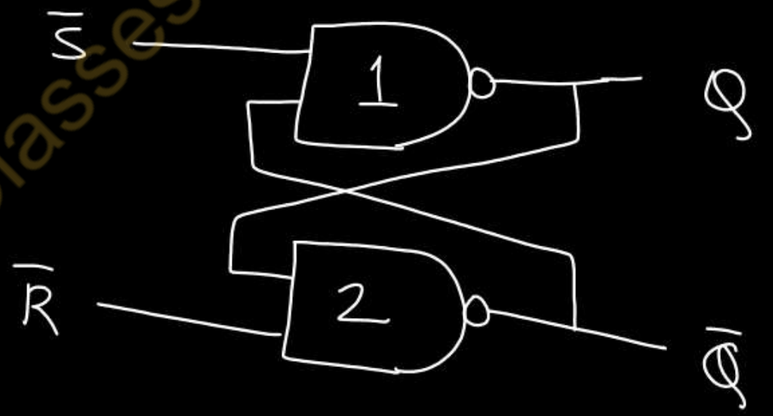
LATCH	FLIP FLOP
latches can be built from gates	flip-flops can be built from latches
latch does not have a clock signal	flip-flop always have a clock signal
latch is a level-triggered type of memory circuit	flip-flop is an edge-triggered type of memory circuit
Latch serve as memory elements in asynchronous sequential circuits.	flip flops serve as memory elements in synchronous sequential Circuits

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Latches

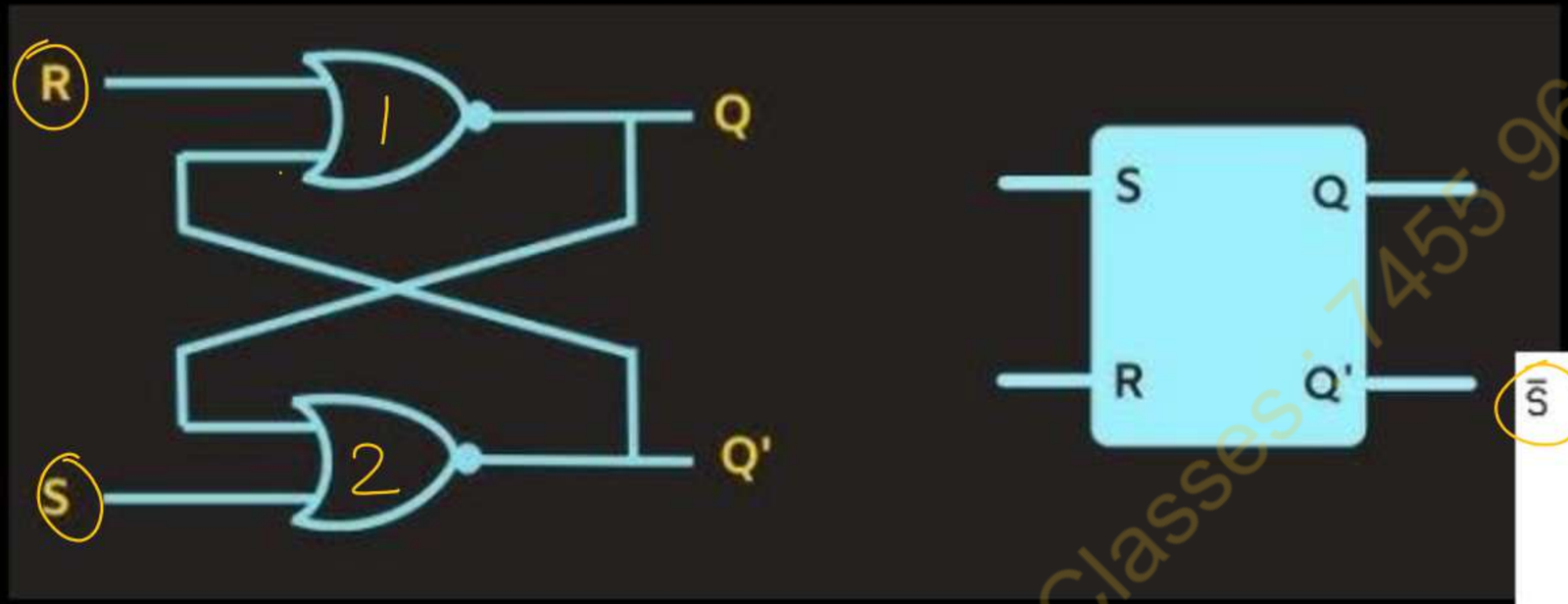
- The circuit shown below is a basic NAND latch.
- The inputs are generally designated "S" and "R" for "Set" and "Reset" respectively.
- The outputs of any single-bit latch or memory are traditionally designated Q and Q'.

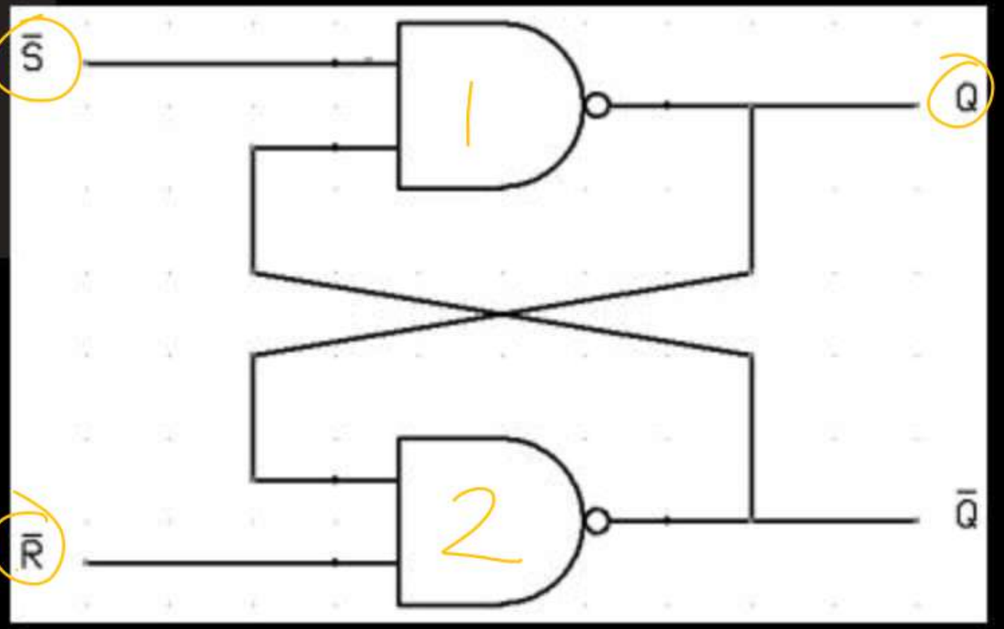




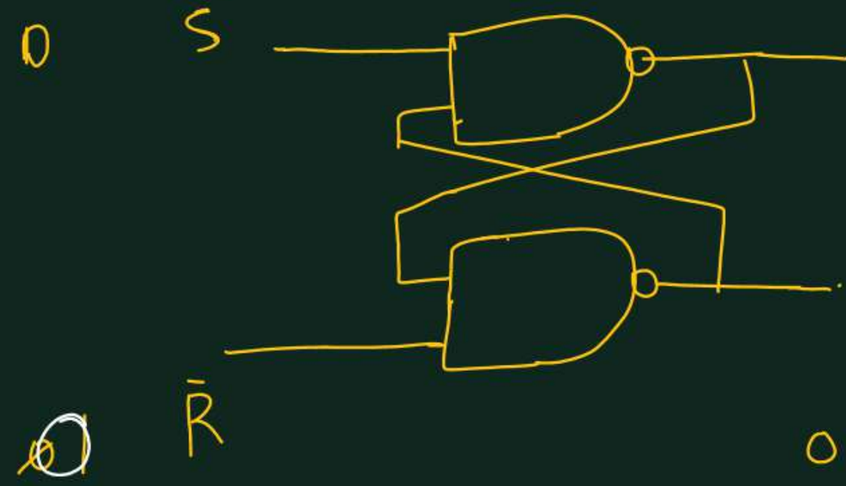
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NAND & NOR LATCH





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$0 \to 1$
$1 \to 1$
$1 \to 1 \to 0$

$0 \to 1$

$1 \to 0$

$0 \to 0$

	$\bar{S}$	$\bar{R}$	S	R	Q_n	$\bar{Q}_n$	Q_{n+1}	$\overline{Q_{n+1}}$
Memory	1	1	0	0	0	1	0	1
	1	1	0	0	1	0	1	0
Reset	1	0	0	1	0	1	0	1
	1	0	0	1	1	0	0	1
Set	0	1	1	0	0	1	1	0
	0	1	1	0	1	0	1	0
Invalid	0	0	1	1	0	1	1	1
	0	0	1	1	1	0	1	1

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UNIVERSITY QUESTIONS

YEAR	QUESTION	MARKS
21-22 20-21	Write the differences between combinational and sequential circuits.	10 Marks 2 Marks
20-21 19-20	What is difference between flip flop and latches?	2 Marks

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DIGITAL SYSTEM DESIGN

UNIT 3 : Sequential logic design

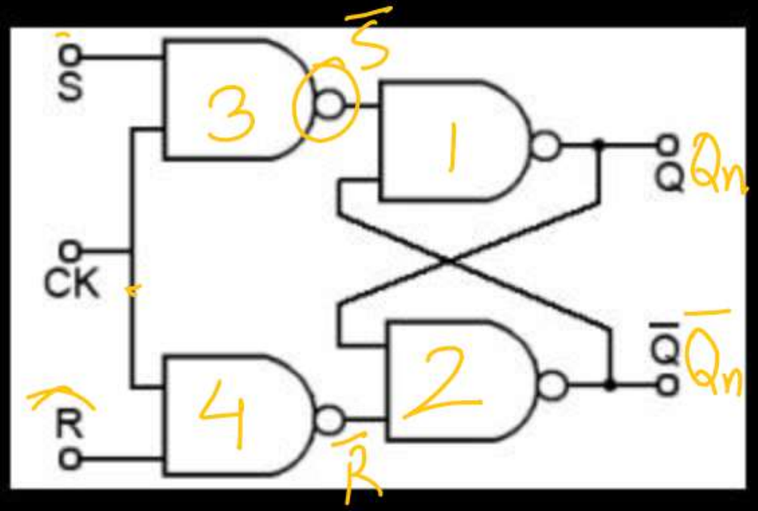
Lec 2

Today's Target

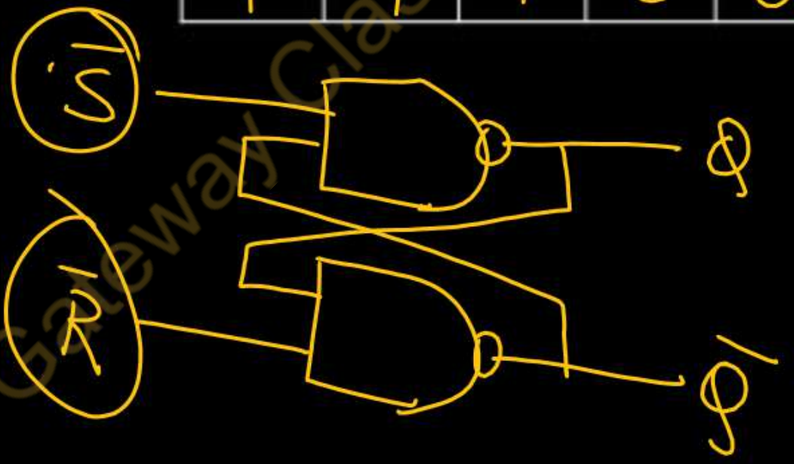
- CLOCKED FLIP FLOP
- D Flip Flop
- J-K Flip Flop
- T Flip Flop
- Race around condition in JK flip-flop
- Master-Slave Flip Flop
- UNIVERSITY QUESTIONS

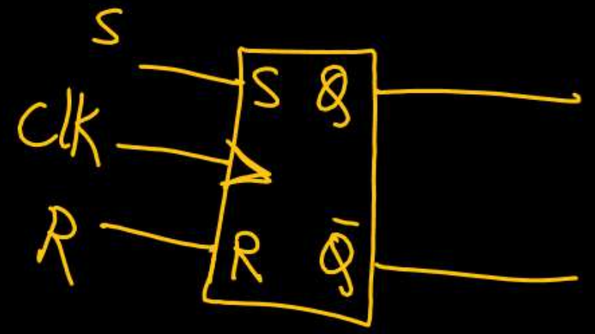
Gateway Classes : 7455 96 10 84

CLOCKED FLIP FLOP



Input					Output		Status of Output
CLK	S	R	S'	R'	Qn+1	Qn+1'	
0	X	X	X	X	Qn	$\overline{Qn}$	No change
1	0	0	1	1	Qn	$\overline{Qn}$	Mem
1	0	1	1	0	0	1	Reset
1	1	0	0	1	1	0	Set
1	1	1	0	0	1	1	Invalid



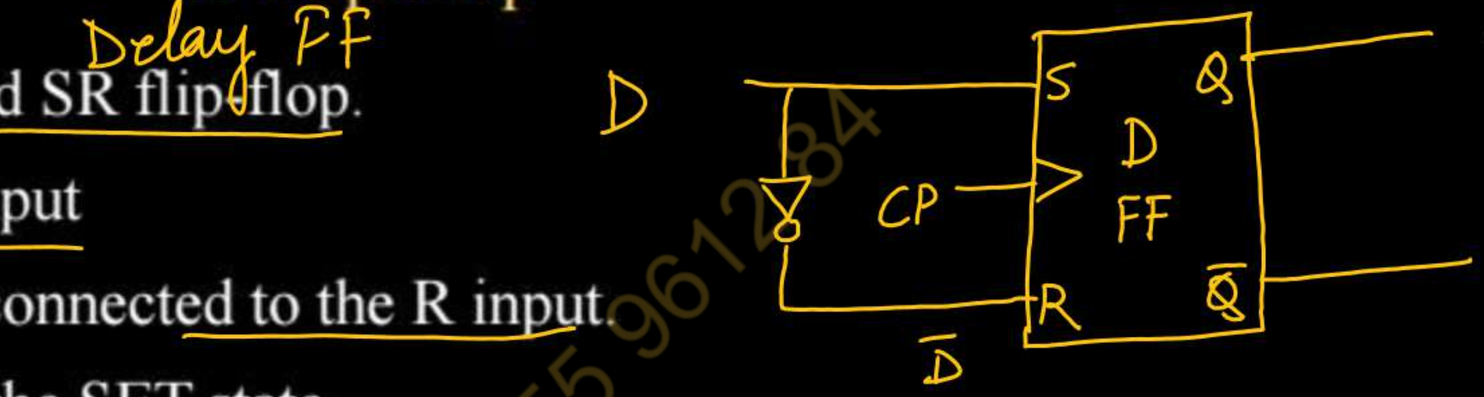


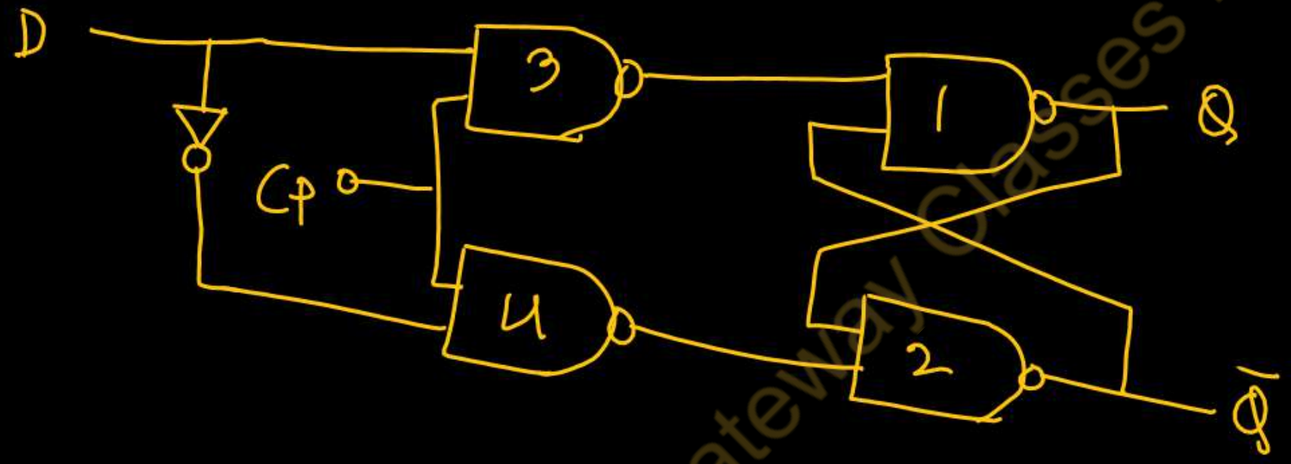
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D Flip Flop

Delay FF

- a slight modification of clocked SR flip-flop.
- D input is connected to the S input
- complement of the D input is connected to the R input.
- When D=1; flip flop moves to the SET state
- When D=0; flip flop switches to the CLEAR state.





Truth Table

CP	D	Qn+1	
0	X	Qn	No change
1	0	0	Reset/Clear
1	1	1	Set

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Timing Diagram



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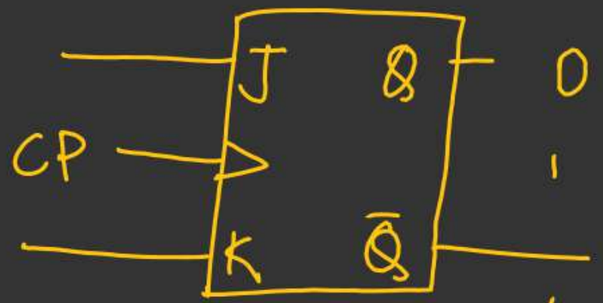
PROBLEM IN SR FF

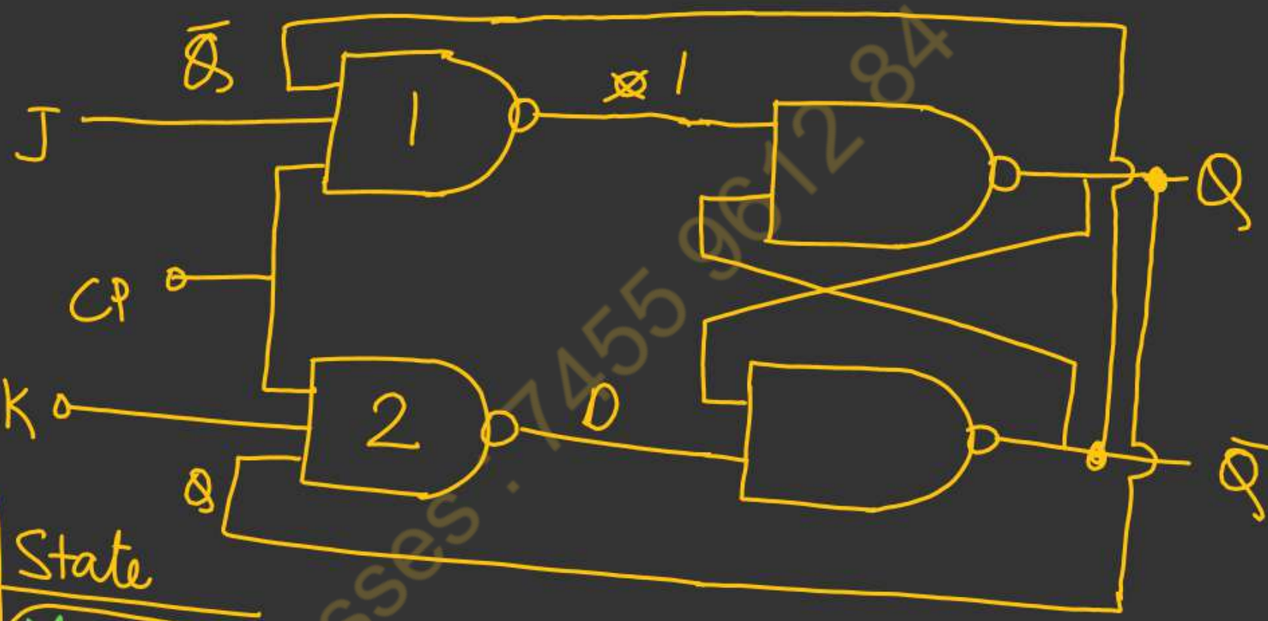
- WHEN S=1: Q=1 (SET STATE)
- WHEN S=0: Q=0 (RESET/CLEAR STATE)
- WHEN S=R=0: Q= PREVIOUS STATE (MEMORY)
- WHEN S=R=1: Q= Q'= 1(INVALID CONDITION)
- To overcome this invalid/ undefined condition, we need to add some more gates.

S	R	Q_{n+1}
0	0	Mem
0	1	0
1	0	1
1	1	Invalid

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JK-FF





0 → 1

1 → 1 → 0

1 → 0

0 → 1

Truth Table

J	K	Q_{n+1}	$\bar{Q}_{n+1}$	State
0	0	Q_n	$\bar{Q}_n$	Memory
0	1	0	1	Reset
1	0	1	0	Set
1	1	$\bar{Q}_n$	Q_n	Complement of Previous o/p

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J-K Flip Flop

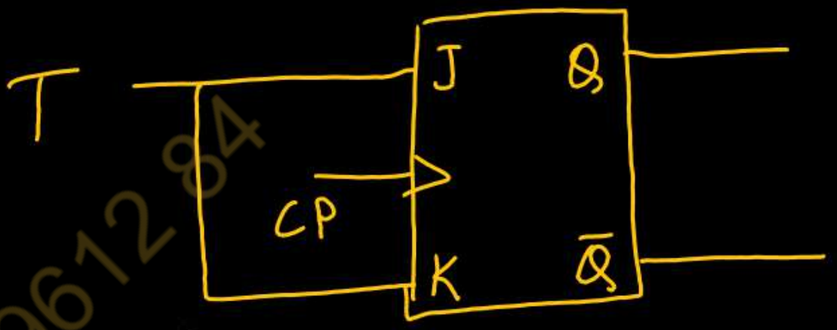
Jack & keying FF

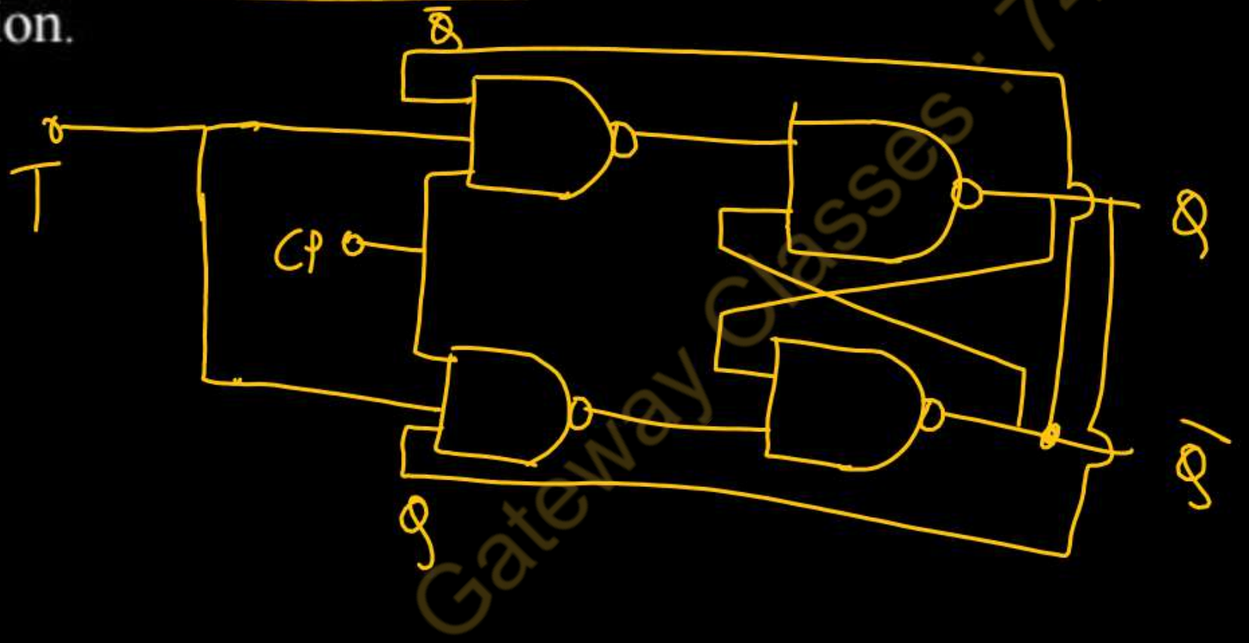
- Also defined as a modification of the S-R flip flop.
- intermediate state is more refined and precise than that of a S-R flip flop.
- J (Jack) resembles S for SET and K(Keying) resembles R for RESET.
- When J=K=1; the flip-flop switch to the complement state
- i.e. for Q = 1, it switches to Q=0 and
  for Q = 0, it switches to Q=1.

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T Flip Flop

- much simpler version of the J-K flip flop
- Both the J and K inputs are connected together
- also called a single input J-K flip flop
- When clock pulse is given to the flip flop, the output begins to toggle
- the restriction on the pulse width can be eliminated with a master-slave or edge-triggered construction.

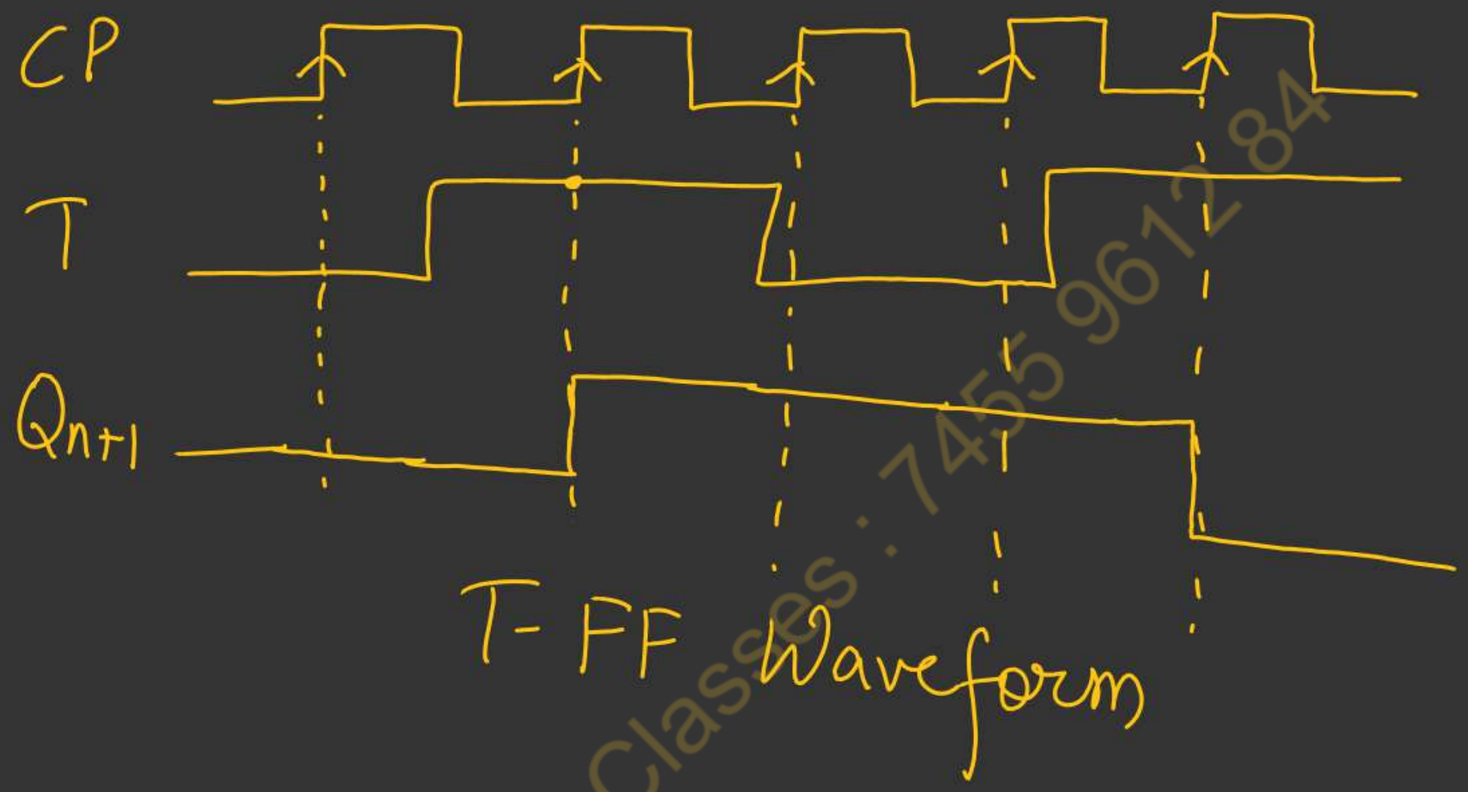




Truth Table

CP	T	Q_{n+1}
0	x	Q_n
1	0	Q_n (Mem)
1	1	$\bar{Q}_n$ (Toggle o/p)

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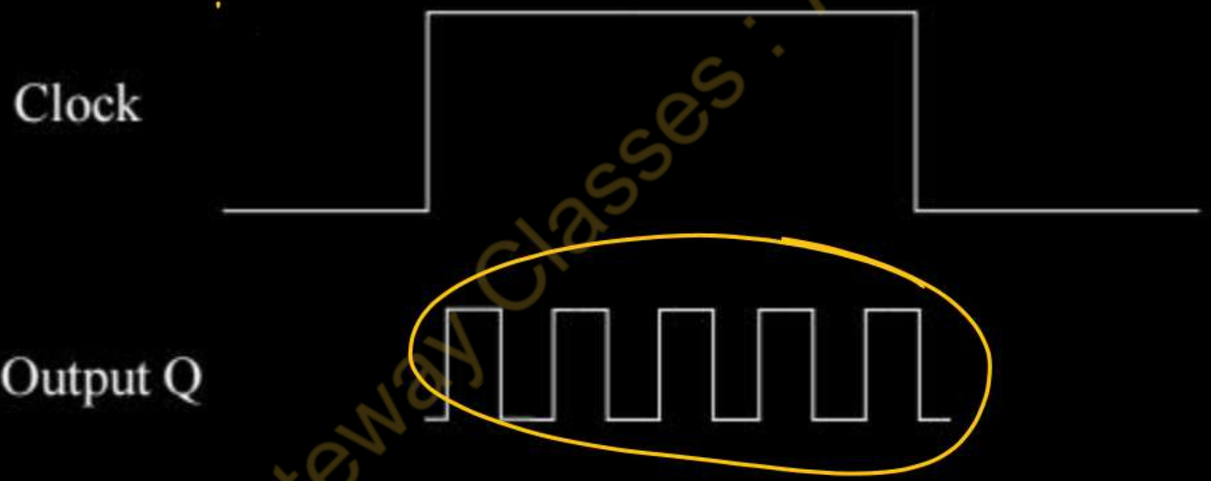


T- FF Waveform

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Race around condition in JK flip-flop:

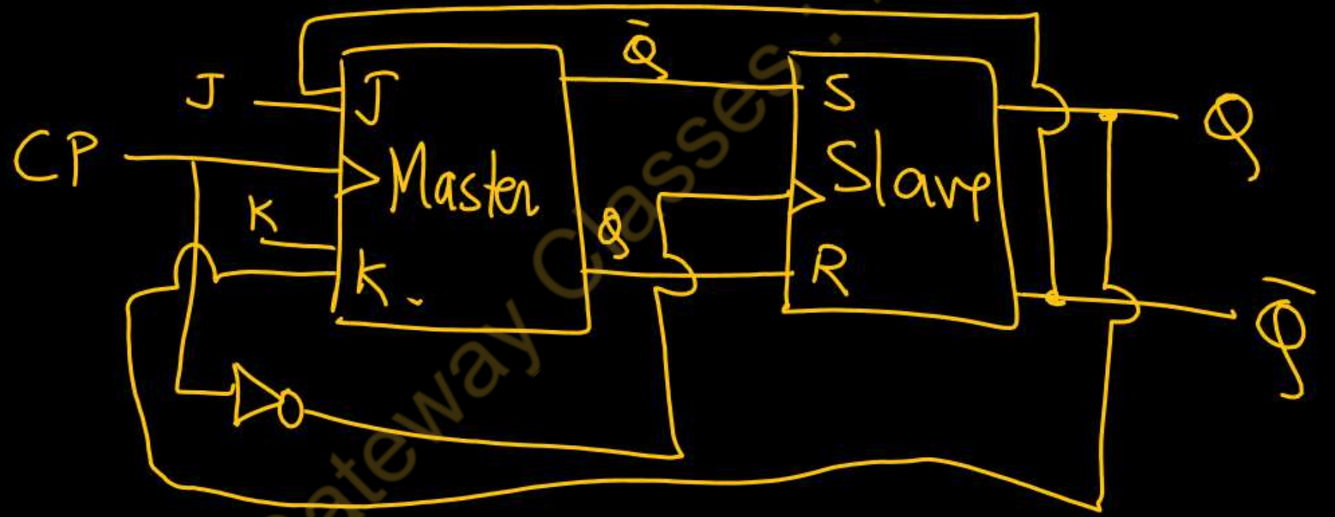
- In JK flip flop as long as clock is high for the input conditions J=K=1
- the output changes or complements its output from 1–>0 and 0–>1.
- This is called toggling output or uncontrolled changing or racing condition.



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Steps to avoid racing condition in JK Flip flop:

- If the Clock On or High time is less than the propagation delay of the flip flop then racing can be avoided.
- This is done by using edge triggering rather than level triggering.
- If the flip flop is made to toggle over one clock period then racing can be avoided.
- This introduced the concept of Master Slave JK flip flop.



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Master-Slave Flip Flop

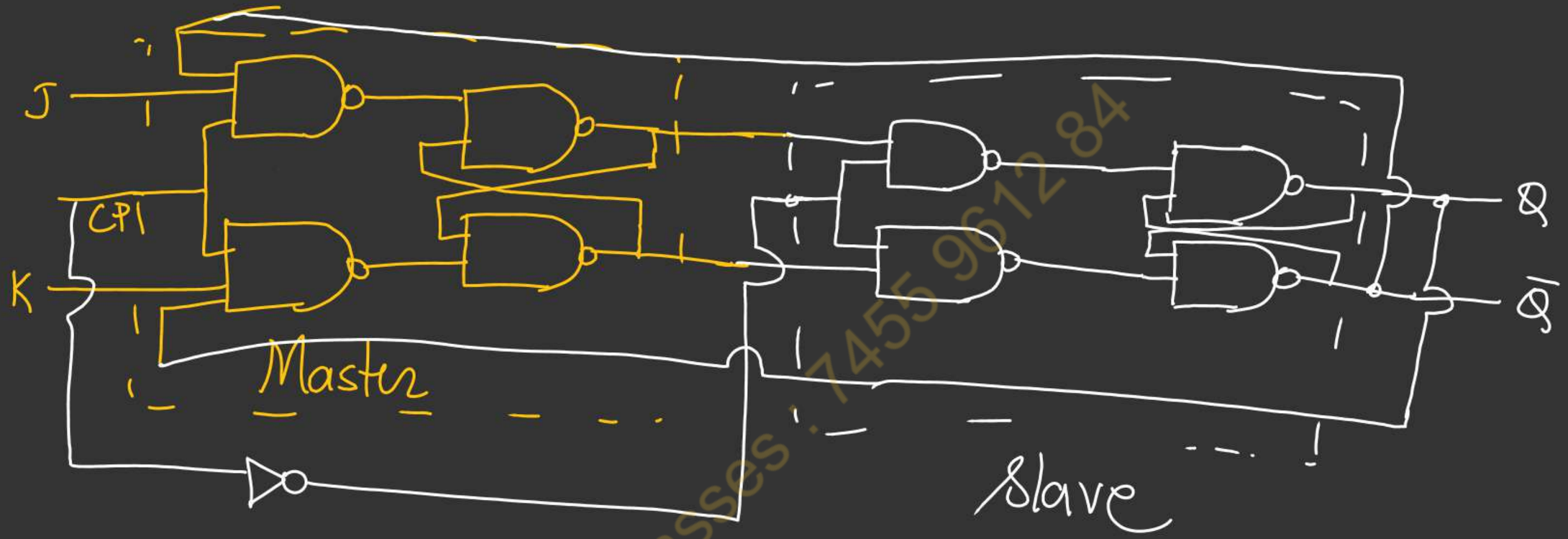
- Master-slave flip flop is designed using two separate flip flops.
- Out of these, one acts as the master and the other as a slave.
- both the J-K flip flops are presented in a series connection.
- The output of the master J-K flip flop is fed to the input of the slave J-K flip flop.
- The output of the slave J-K flip flop is given as a feedback to the input of the master J-K flip flop.
- The clock pulse [Clk] is given to the master J-K flip flop and it is sent inverted to the slave J-K flip flop.

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Working of M-S FF

- When Clk=1, the master J-K flip flop gets disabled. enabled
- The Clk input of the master input will be the opposite of the slave input.
- So the master flip flop output will be recognized by the slave flip flop only when the Clk value becomes 0.
- when the clock pulse males a transition from 1 to 0, the locked outputs of the master flip flop are fed through to the inputs of the slave flip-flop making this flip flop edge or pulse-triggered.

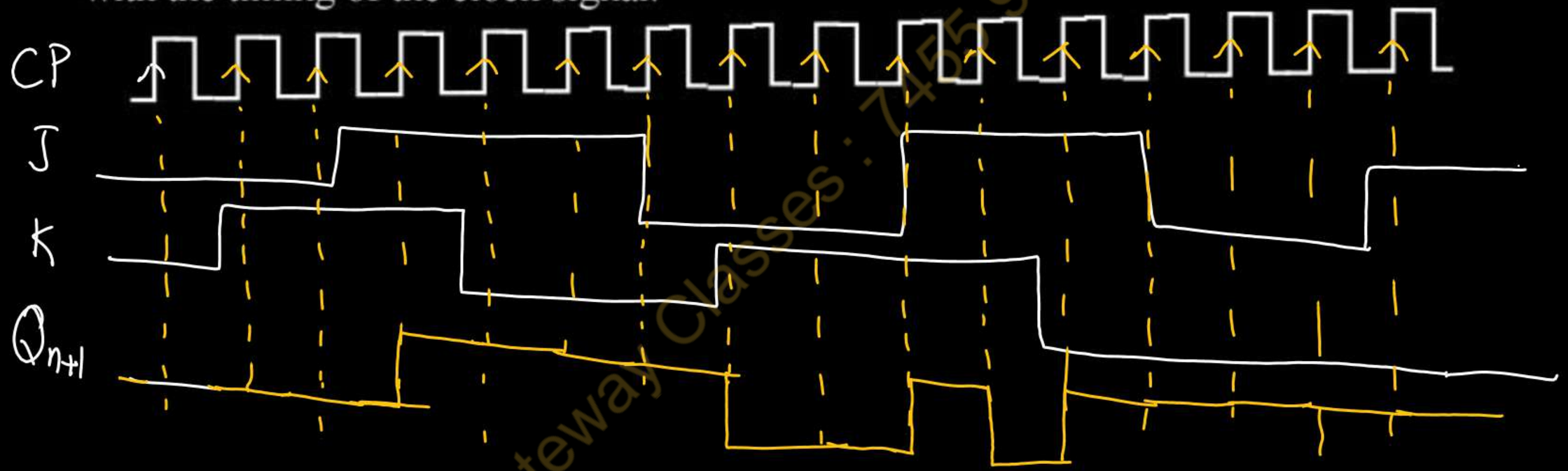
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TIMING DIAGRAM

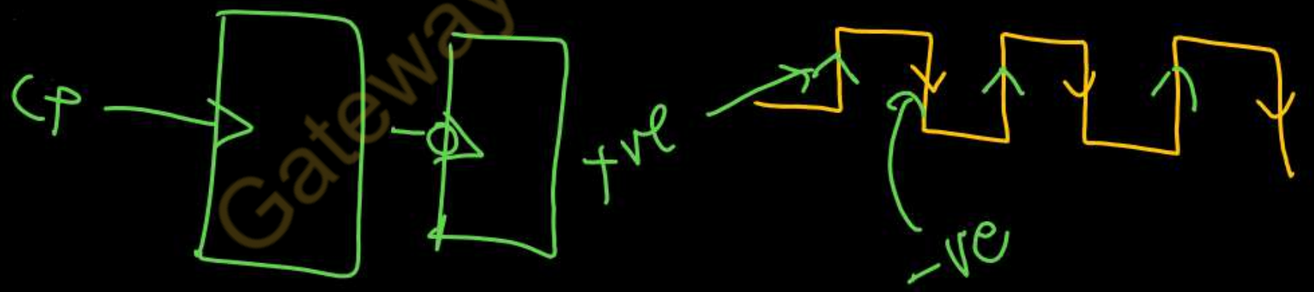
- The circuit accepts the value in the input when the clock is HIGH, and passes the data to the output on the falling-edge of the clock signal.
- This makes the Master-Slave J-K flip flop a Synchronous device as it only passes data with the timing of the clock signal.



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UNIVERSITY QUESTIONS

YEAR	QUESTIONS	MARKS
22-23, 19-20	What do you mean by race around condition in JK Flip Flop?	2 Marks
21-22	Explain the working of Master-Slave JK flip-flop with the help of logic diagram, functional table, logic symbol.	10 Marks
21-22	Explain positive edge triggered D-flip-flop with the help of circuit diagram and waveforms.	10 Marks



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DIGITAL SYSTEM DESIGN

UNIT 3 : Sequential logic design

Lec 3

Today's Target

- Preset and Clear inputs of flip flop
- Digital Registers
- Bidirectional Shift Registers
- Universal Shift Register
- University Questions

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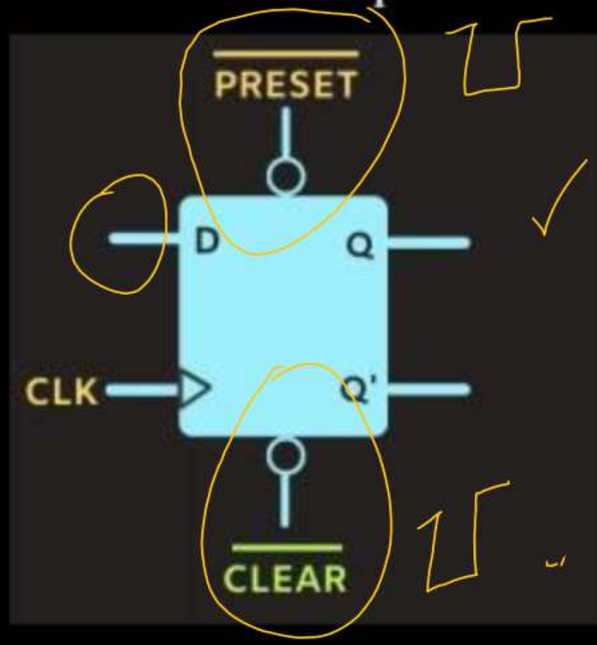
UNIVERSITY QUESTIONS

YEAR	QUESTIONS	MARKS
21-22	Distinguish between shifter and barrel shifter?	2 Marks
21-22	What do you mean by shift register? What is the need of shift register? Draw and explain bidirectional shift register.	7 Marks

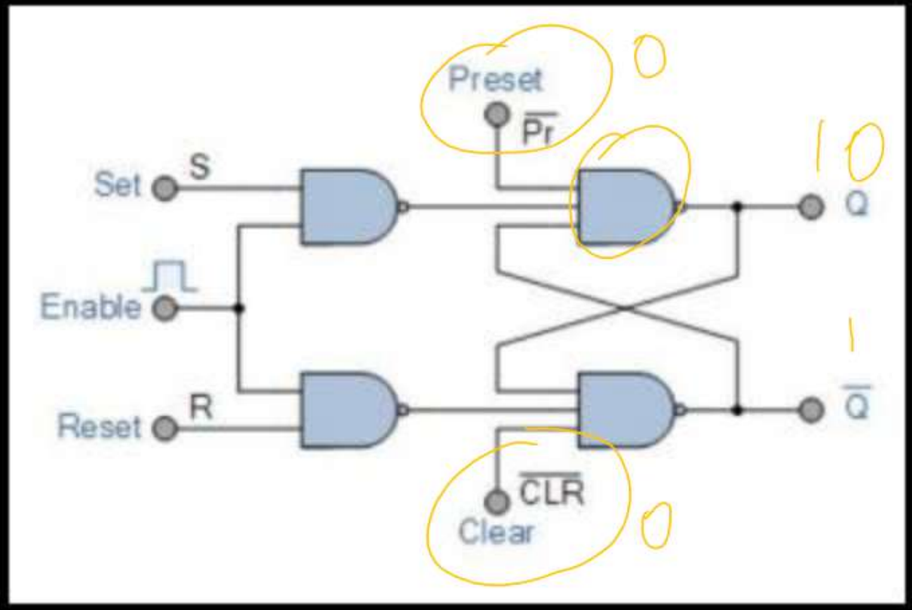
Gateway Classes: 1455 9612 84

Preset and Clear inputs of flip flop

- Preset and clear inputs are called **Asynchronous inputs** as they act on the flip flop independent of the clock.
- The preset input is used to set the Flip flop to 1
- The clear input is used to set the Flip flop to 0
- If both preset and clear is low at the same time, the o/p of flip flop states becomes X. (Don't Care)
- If both preset and clear is high at the same time, the o/p of flip flop is controlled by clock and JK inputs



CLK	PRE	CLR	D	Q n+1
X	0	0	X	Invalid
X	0	1	X	1
X	1	0	X	0
0	1	1	X	Q n
↑	1	1	0	0
↑	1	1	1	1

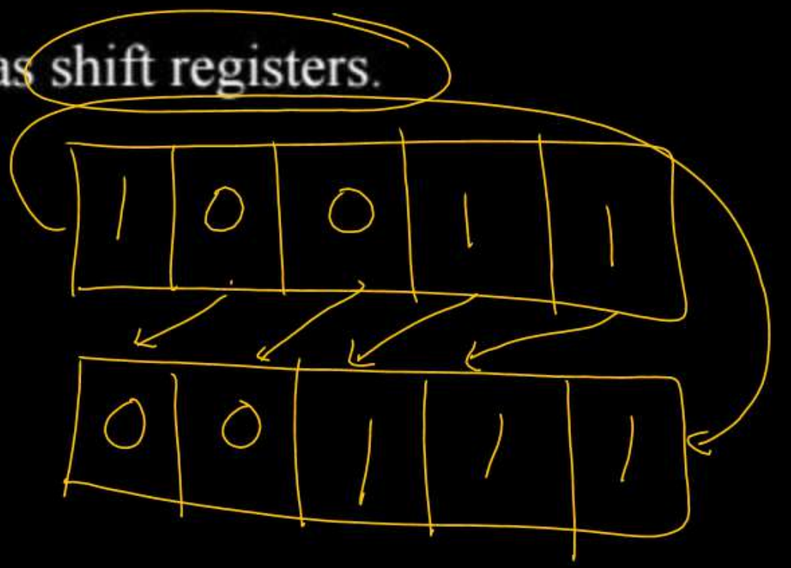


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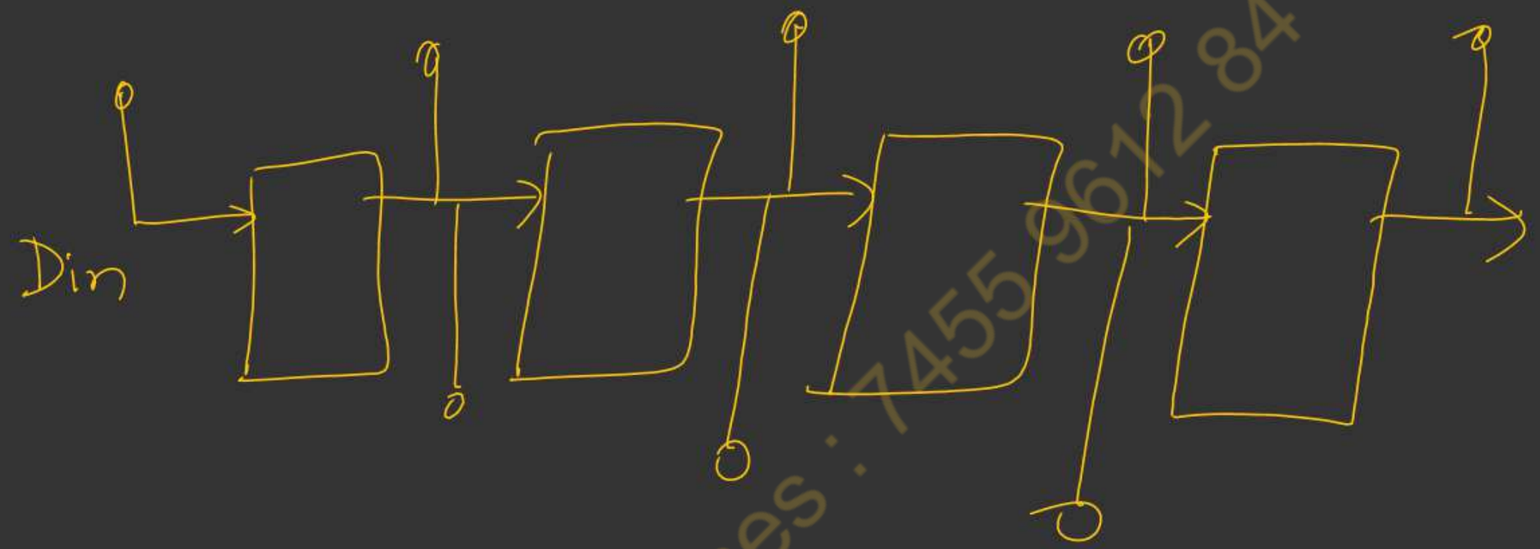
Digital Registers

Shift Register

- Flip-flop is a 1 bit memory cell which can be used for storing the digital data.
- To increase the storage capacity in terms of number of bits, we have to use a group of flip-flop. Such a group of flip-flop is known as a Register.
- The n-bit register will consist of n number of flip-flop and it is capable of storing an n-bit word.
- The binary data in a register can be moved within the register from one flip-flop to another.
- The registers that allow such data transfers are called as shift registers.
- There are four mode of operations of a shift register.
- Serial Input Serial Output — SISO
- Serial Input Parallel Output — SIPO
- Parallel Input Serial Output — PISO
- Parallel Input Parallel Output — PIPO

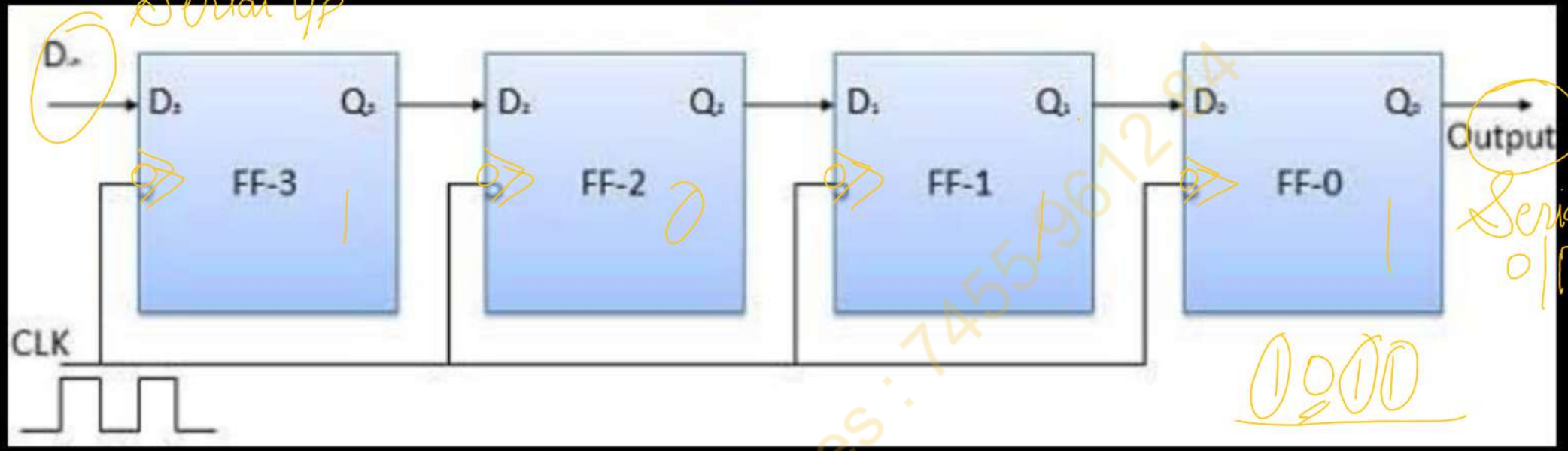


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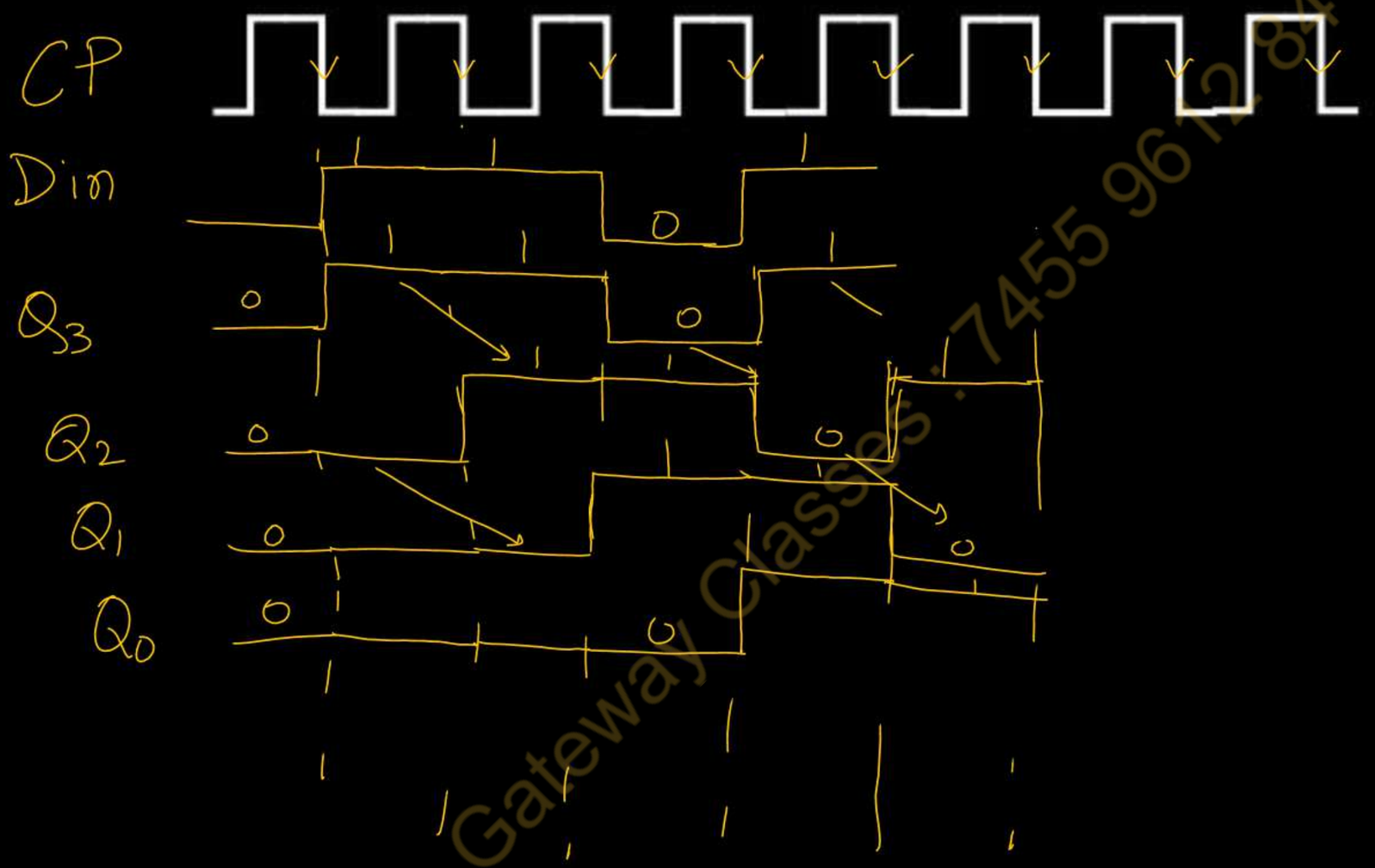
Block Diagram & Truth Table



Initially	CLK	D_{in}	Q_3	Q_2	Q_1	Q_0
			0	0	0	0
(i)	↓	1	1	0	0	0
(ii)	↓	1	1	1	0	0
(iii)	↓	0	0	1	1	0
(iv)	↓	1	1	0	1	1

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Waveforms



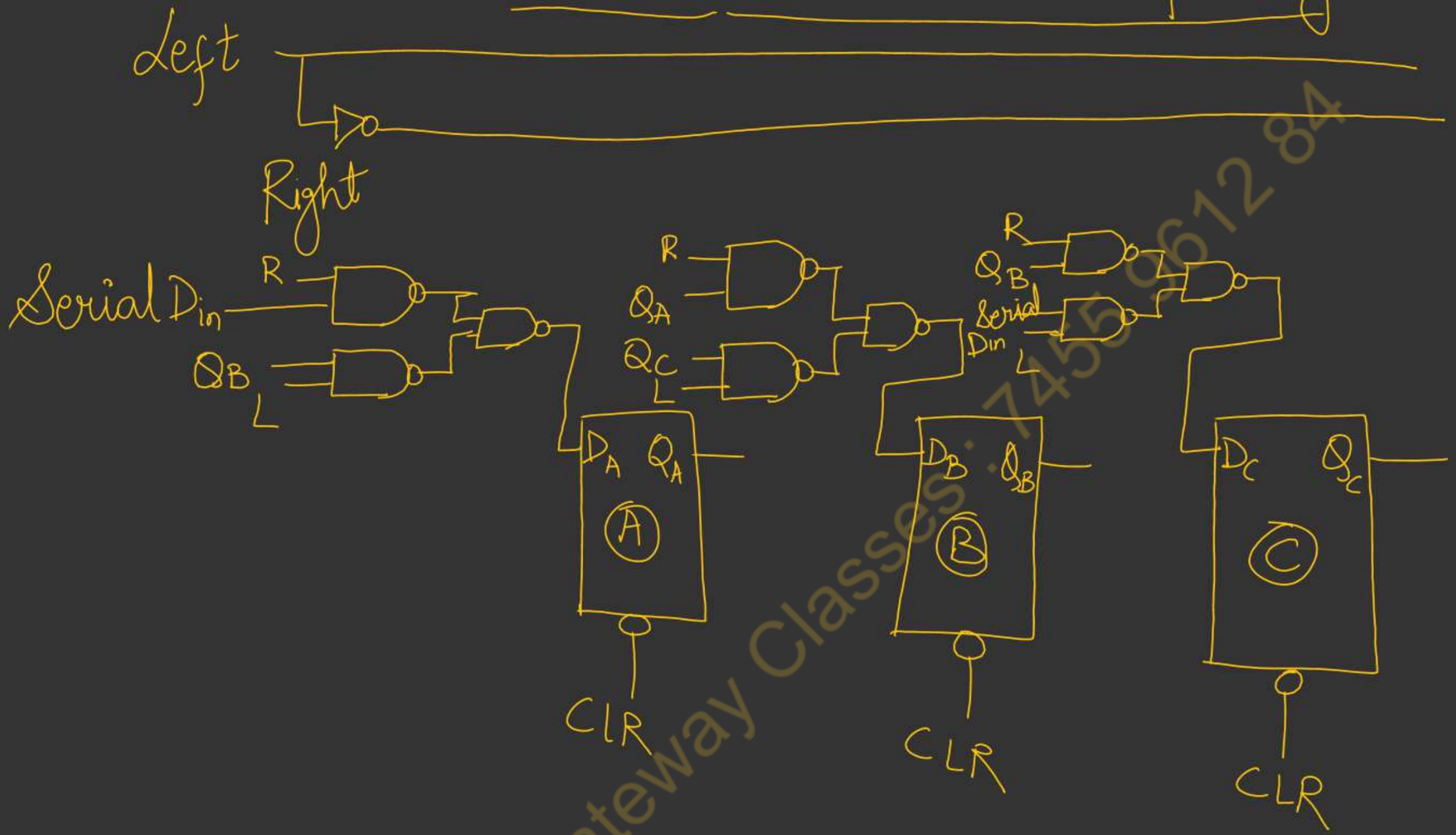
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Bidirectional Shift Registers

- Shift registers could either perform right or left data shift, or both depending on the kind of shift register and their configuration.
- In right shift operations, the binary data is divided by two.
- If this operation is reversed, the binary data gets multiplied by two.
- With suitable application of combinational logic, a serial shift register can be configured to perform both operation.
- The control line left/write is used to determine the direction to which data is shifted, either right or left.

Gateway Classes : 1455 9612 84

3 Bit Bidirectional Shift Reg

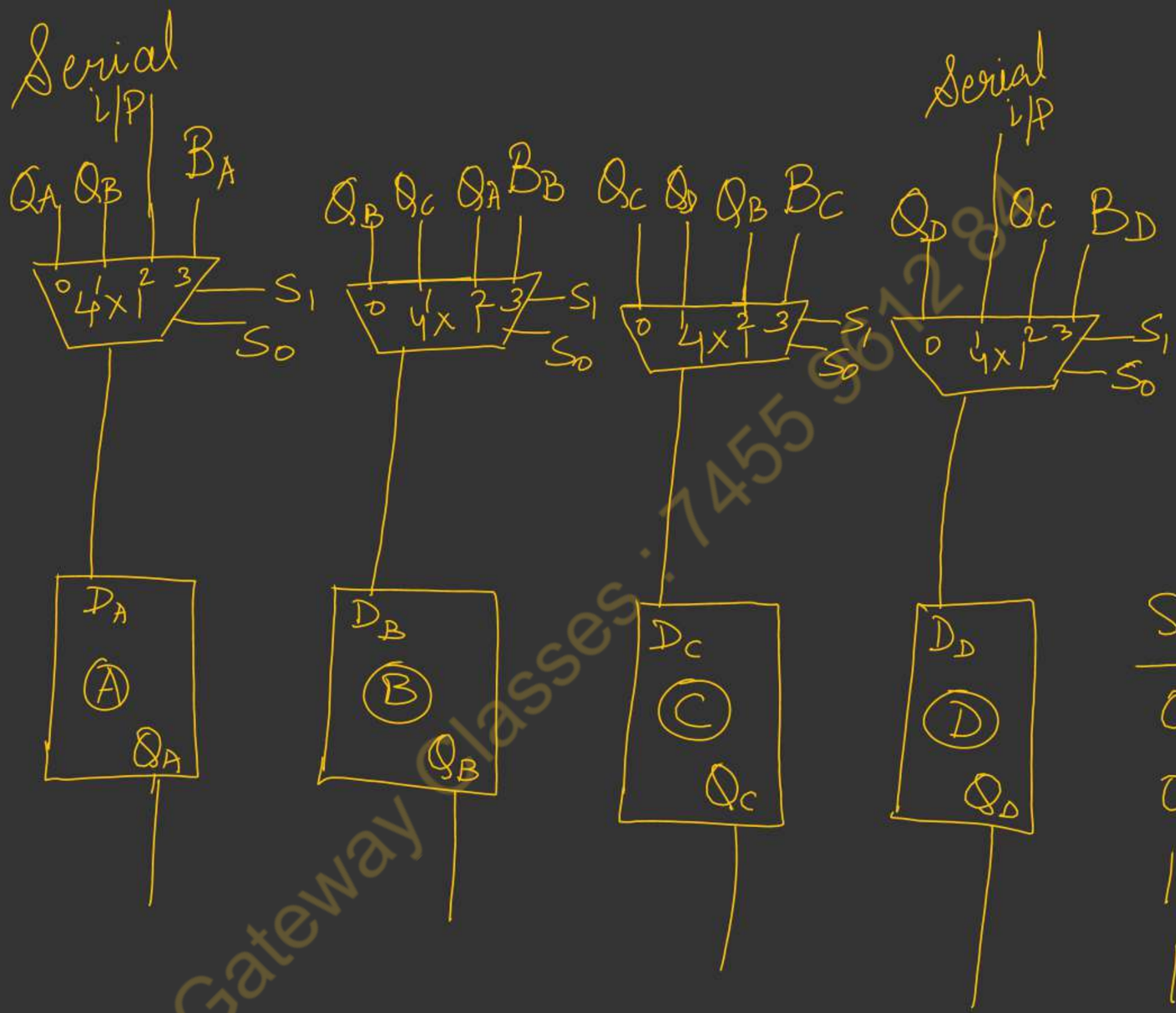


Gateway Classes: 7455961284

Universal Shift Register

- A Universal shift register is a register which has both the right shift and left shift with parallel load capabilities.
- Universal shift registers are used as memory elements in computers.

Gateway Classes : 7455 96 12 84



S_1	S_0	Operation
0	0	No change
0	1	Left Shift
1	0	Right Shift
1	1	Parallel Load

Gateway Classes: 7455 961281

DIGITAL SYSTEM DESIGN

UNIT 3 : Sequential logic design
Lec 4

Today's Target

- Counters
- Asynchronous or Ripple Counters (UP & DOWN Counter)
- Synchronous counters (UP & DOWN Counter)
- University Questions

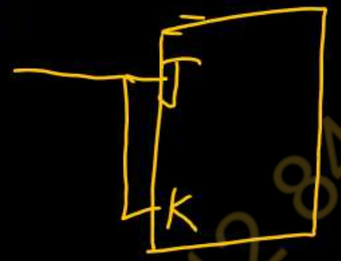
Gateway Classes : 7455 9612 84

UNIVERSITY QUESTIONS

YEAR	QUESTIONS	MARKS
21-22	Write the difference between ripple counter and synchronous counter	5 Marks
20-21	Design and implement a synchronous 3-bit up/down counter using JK flip-flops.	10 Marks
18-19	Design a ripple decade counter using JK flip	7 Marks

Gateway Classes : 1455 9612 84

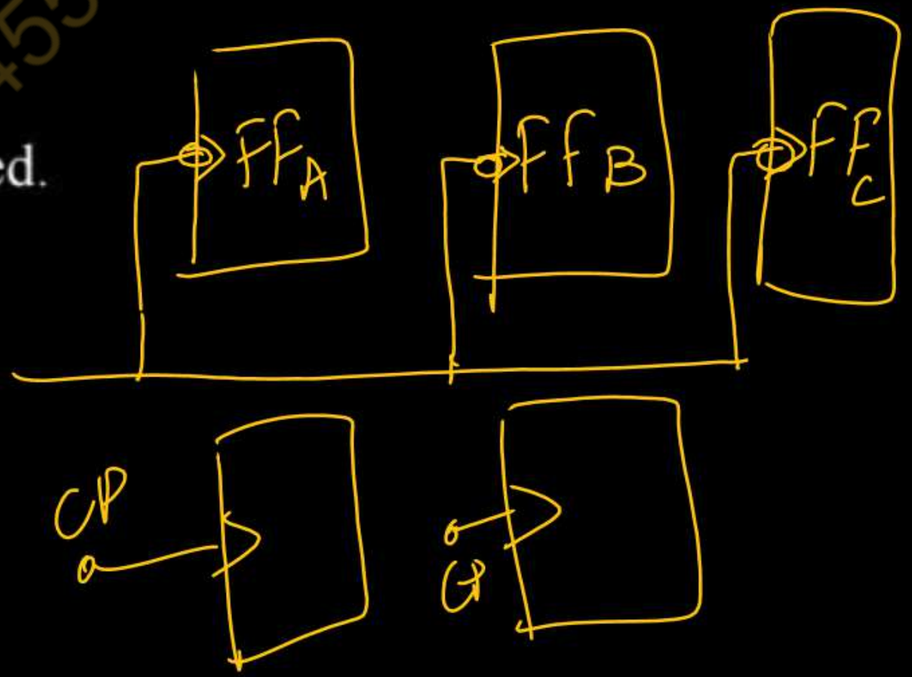
Counters



- Counter is a sequential circuit.
- A digital circuit which is used for a counting pulses is known counter.
- Counter is the widest application of flip-flops.
- It is a group of flip-flops with a clock signal applied.
- Counters are of two types.

1) Asynchronous or ripple counters.

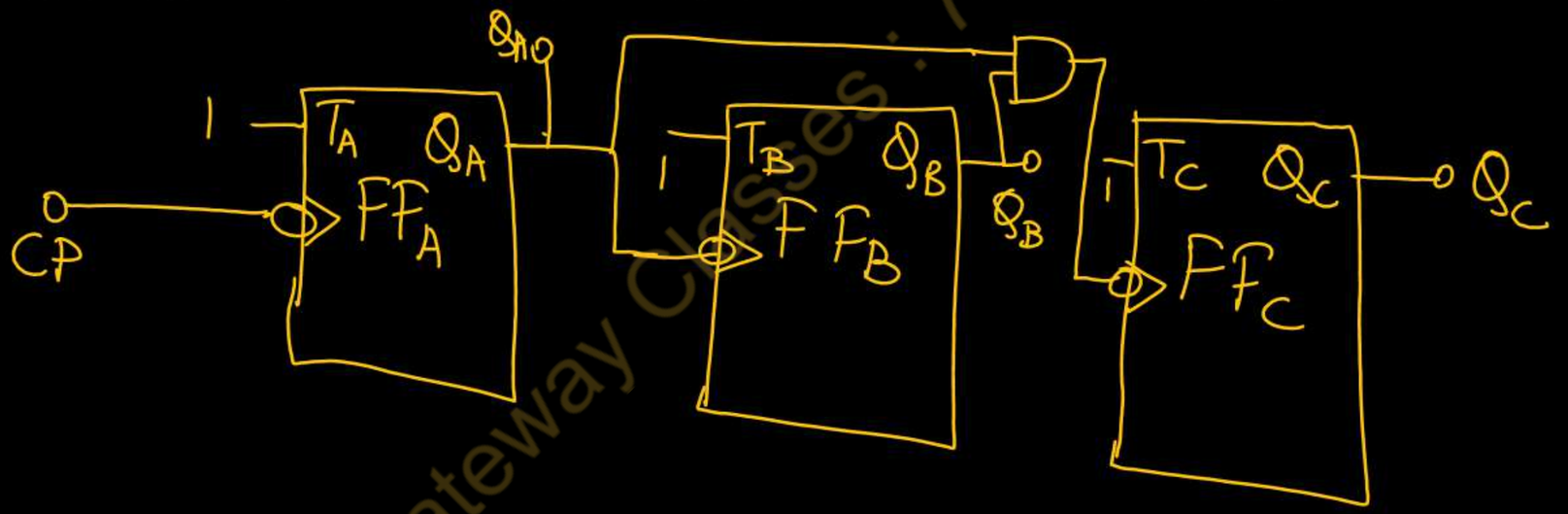
2) Synchronous counters.



Gateway Classes: 7455 961284

Asynchronous or Ripple Counters

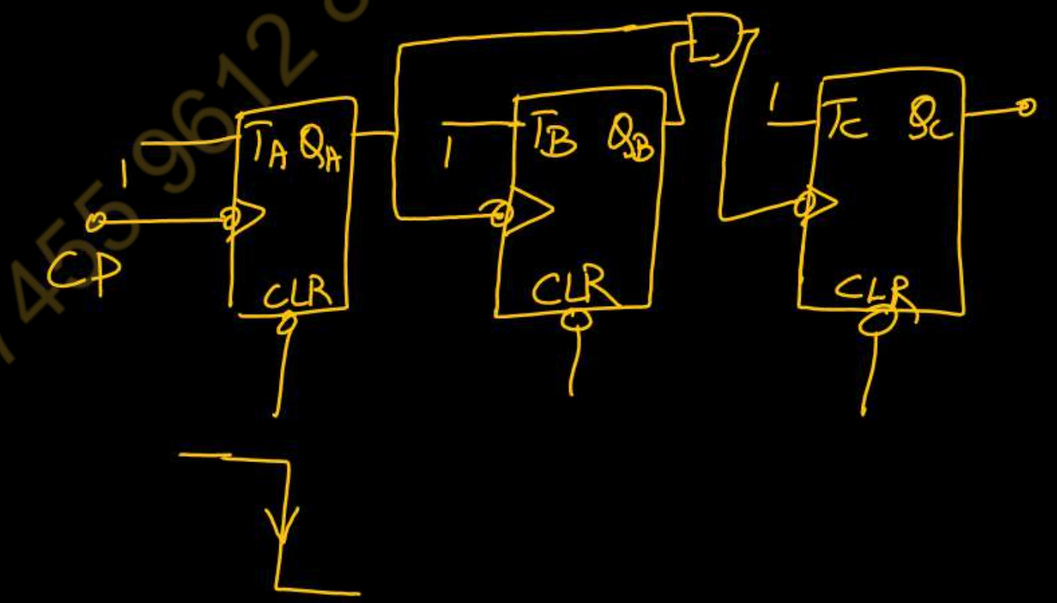
- The toggle (T) flip-flop are being used.
- External clock is applied to the clock input of flip-flop A and QA output is applied to the clock input of the next flip-flop i.e. FF-B and QB output is applied to the clock input of the next flip-flop i.e. FF-C
- The logic diagram of a 3-bit ripple up counter is shown below.



Gateway Classes : 7455 9619 84

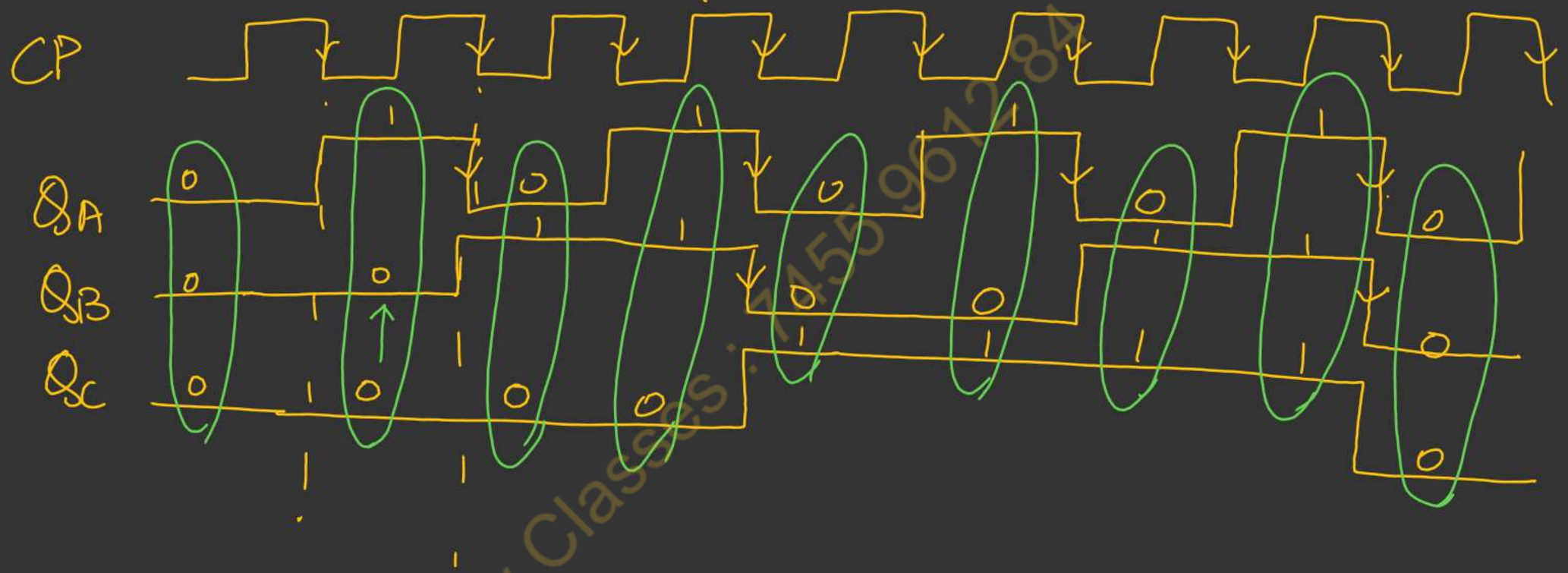
Truth Table

CLK	Counter Output			State Number	Decimal Number
	QC	QB	QA		
Initially	0	0	0	1	0
1st	0	0	1	2	1
2nd	0	1	0	3	2
3rd	0	1	1	4	3
4th	1	0	0	5	4
5th	1	0	1	6	5
6th	1	1	0	7	6
7th	1	1	1	8	7
8th	0	0	0	1	0



Gateway Classes : 7455961284

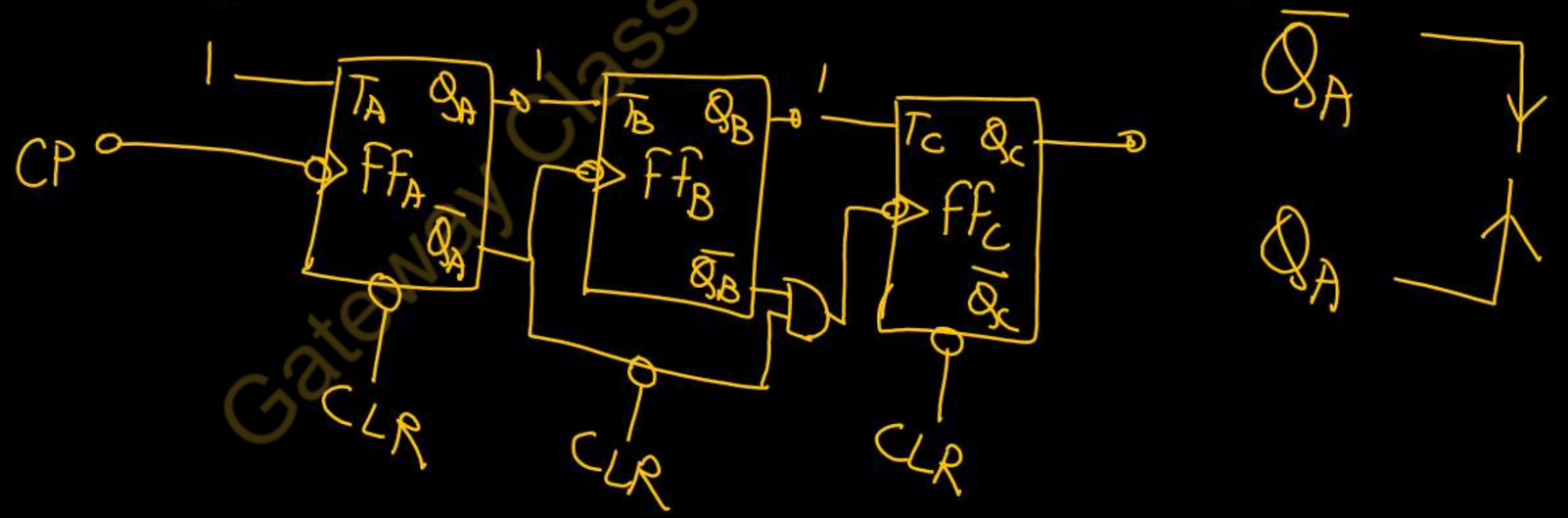
Waveform



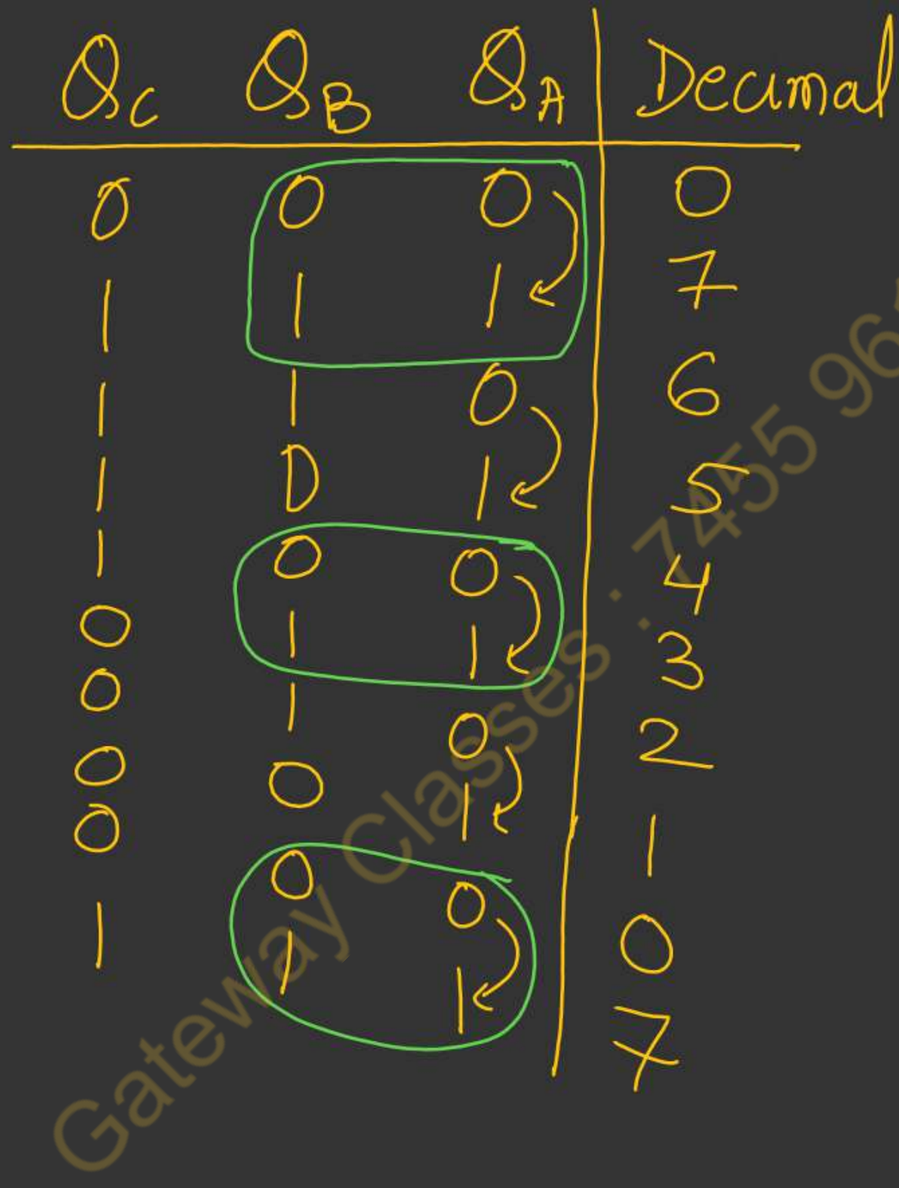
Gateway Classes : 7455961284

Asynchronous Binary Down Counter

- consists of 'N' T flip-flops.
- It counts from $2^N - 1$ to 0.
- The block diagram of 3-bit Asynchronous binary down counter is shown in the following figure.
- Assume the initial status of T flip-flops from rightmost to leftmost is Q2Q1Q0=000
- QA toggled for every negative edge of clock signal.
- QB toggles when Q0 goes from 0 to 1, otherwise remained in the previous state.
- Q2 toggles when Q1 that goes from 0 to 1, otherwise remained in the previous state.

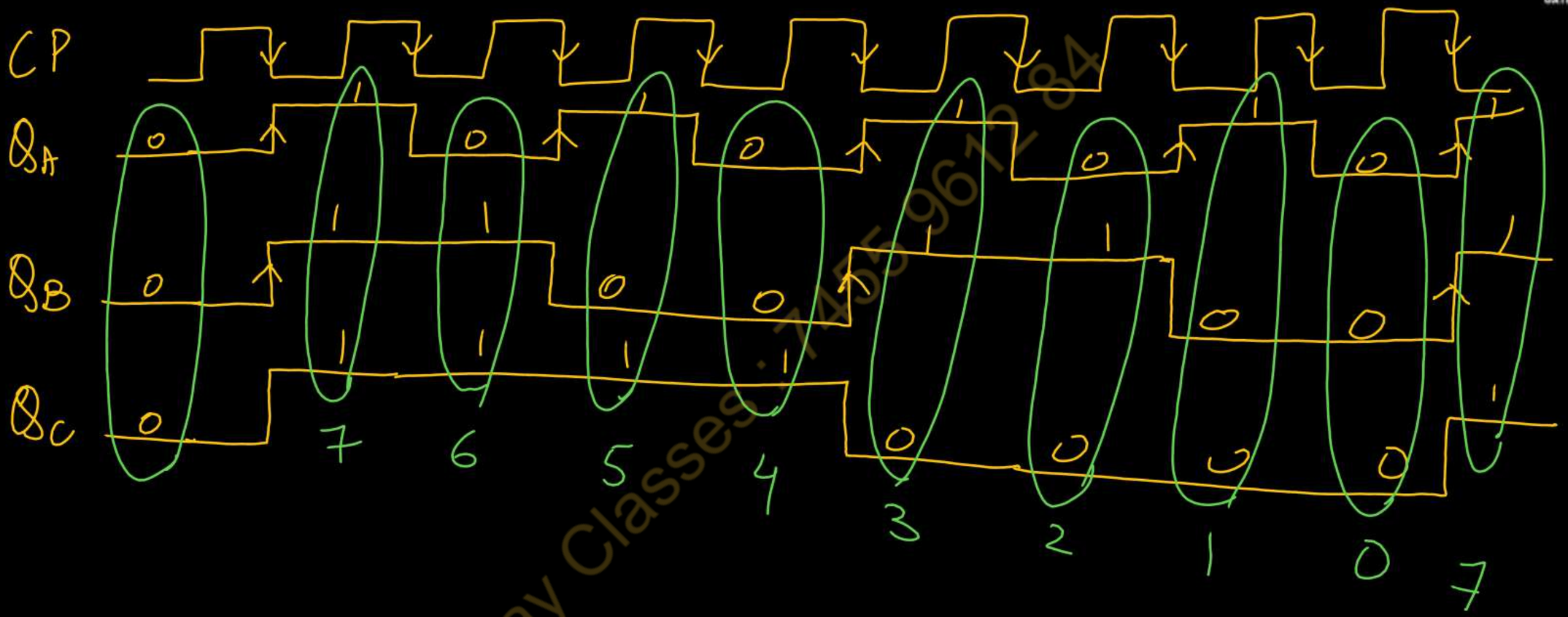


Gateway Classes : 7455 9612 84



Gateway Classes : 7455 9612 84

Waveforms

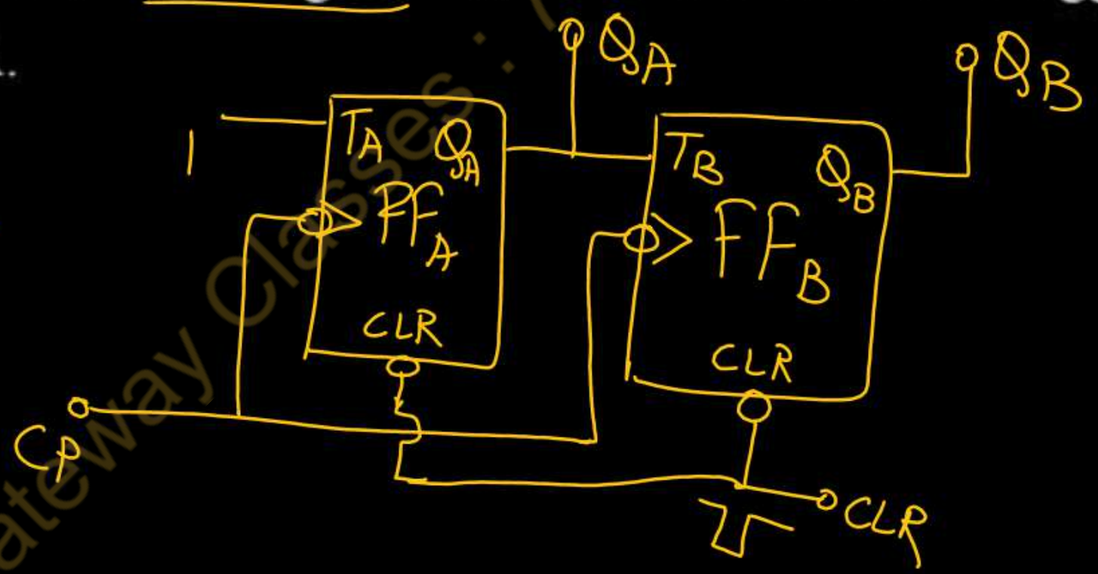


Gateway Classes: 7405 9612 84

2 bit Synchronous counters

- If the "clock" pulses are applied to all the flip-flops in a counter simultaneously, then such a counter is called as synchronous counter.
- 2-bit Synchronous up counter
- The JA and KA inputs of FF-A are tied to logic 1. So FF-A will work as a toggle flip-flop. The JB and KB inputs are connected to QA.

CLR	Q_B	Q_A	Dec
Initial	0	0	0
↓	0	1	1
↓	1	0	2
↓	1	1	3
↓	0	0	0

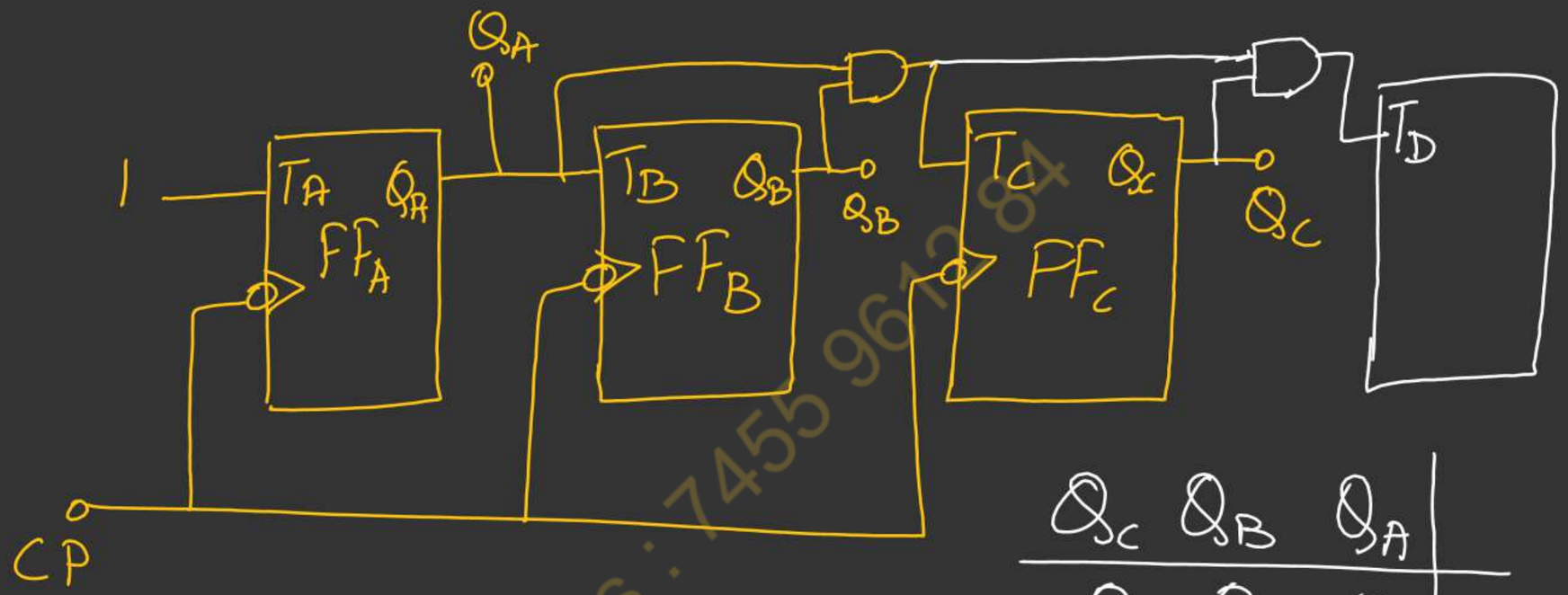


Gateway Classes : 7455 961284

3 bit Synchronous Binary Up Counter

- Contains three T flip-flops & one 2-input AND gate.
- All flip-flops are negative edge triggered
- outputs of flip-flops change synchronously
- T inputs of first, second and third flip-flops are 1
- The output of first T flip-flop toggles for every negative edge of clock signal
- The output of second T flip-flop toggles for every negative edge of clock signal if Q0=1
- The output of third T flip-flop toggles for every negative edge of clock signal if both Q0 & Q1 are 1.

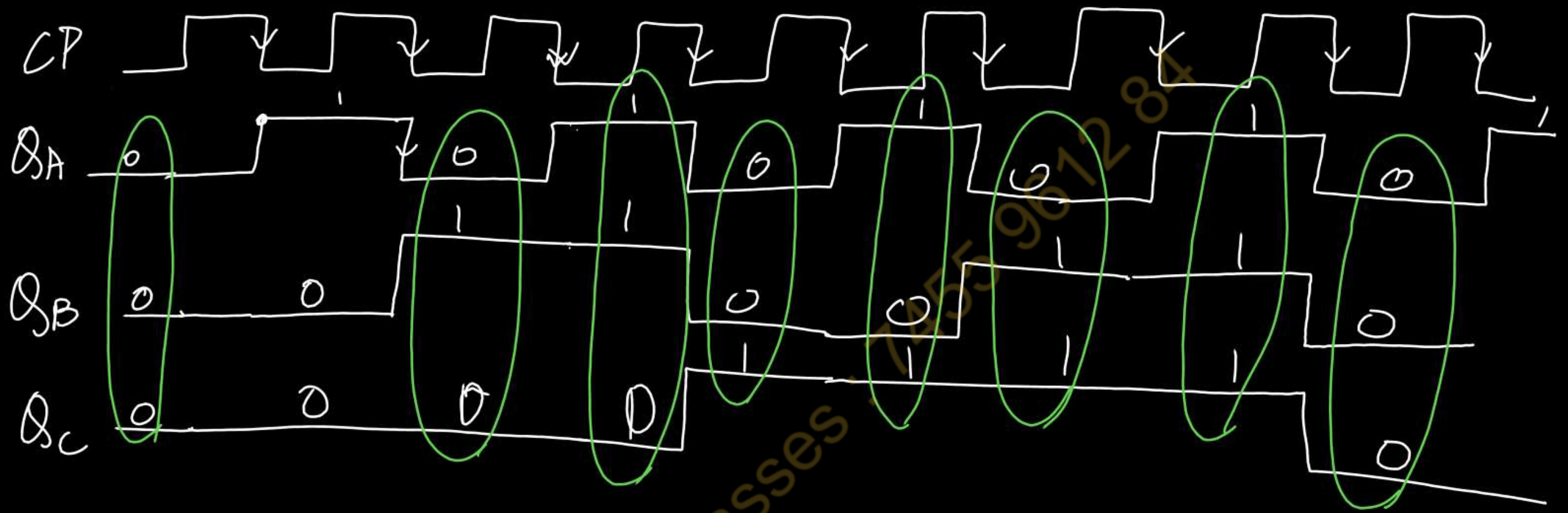
Gateway Classes : 7455 9612 84



Q_C	Q_B	Q_A
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Gateway Classes : 7455 961 284

Waveforms

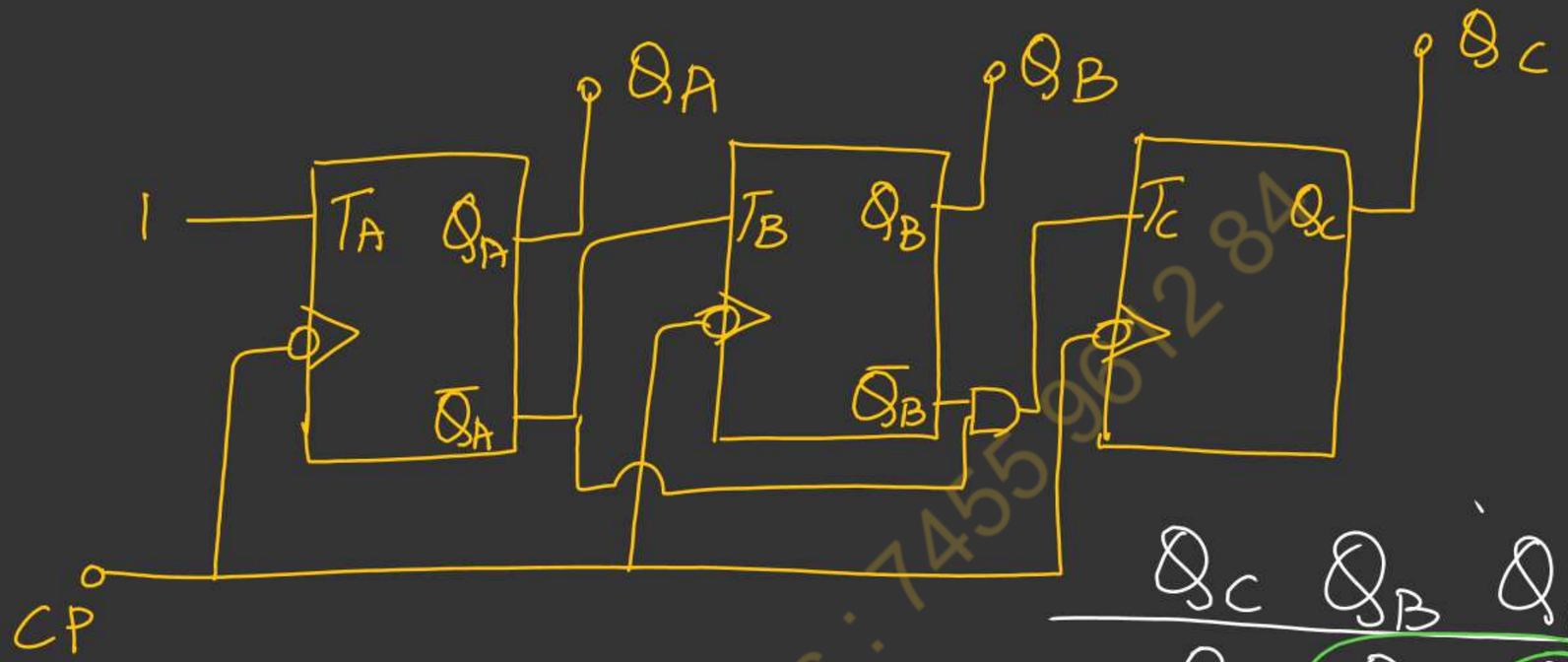


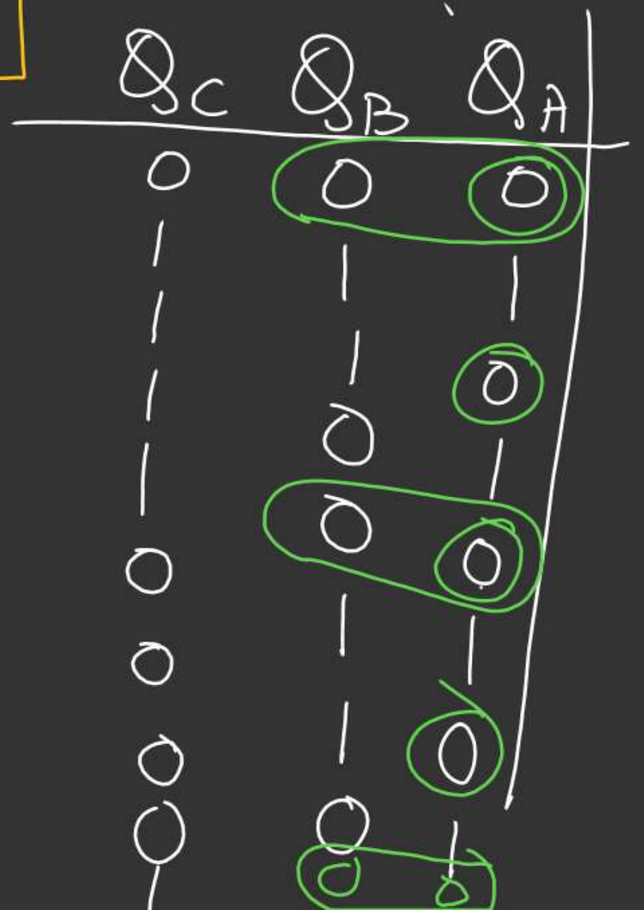
Gateway Classes +91 95 9612 84

3 bit Synchronous Binary Down Counter

- contains three T flip-flops & one 2-input AND gate
- All these flip-flops are negative edge triggered
- outputs of flip-flops change synchronously.
- T inputs of first, second and third flip-flops are 1
- The output of first T flip-flop **toggles** for every negative edge of clock signal.
- The output of second T flip-flop toggles for every negative edge of clock signal if Q0′=1.
- The output of third T flip-flop toggles for every negative edge of clock signal if both Q1′ & Q0′ are 1.

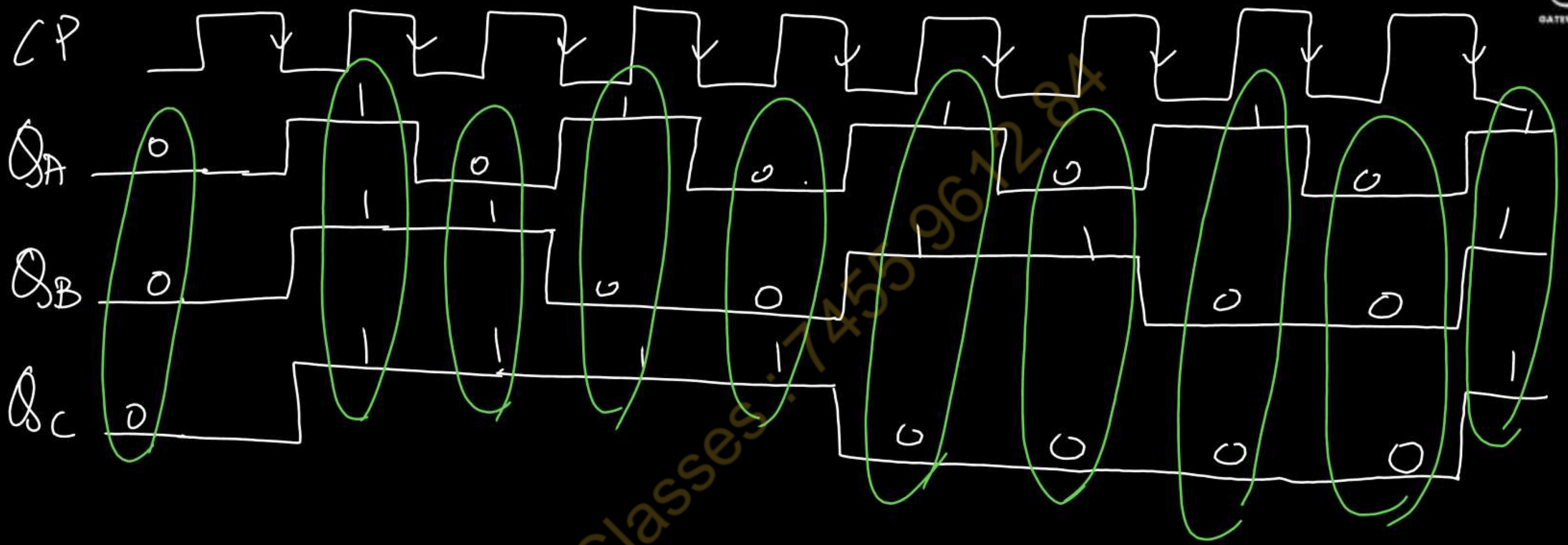
Gateway Classes: 7455 9612 84





Gateway Classes : 7455962 84

Waveforms



Gateway Classes: 7455 96128 4

DIGITAL SYSTEM DESIGN

UNIT 3 : Sequential logic design

Lec 5

Gateway Classes : 7455 961 284

Today's Target

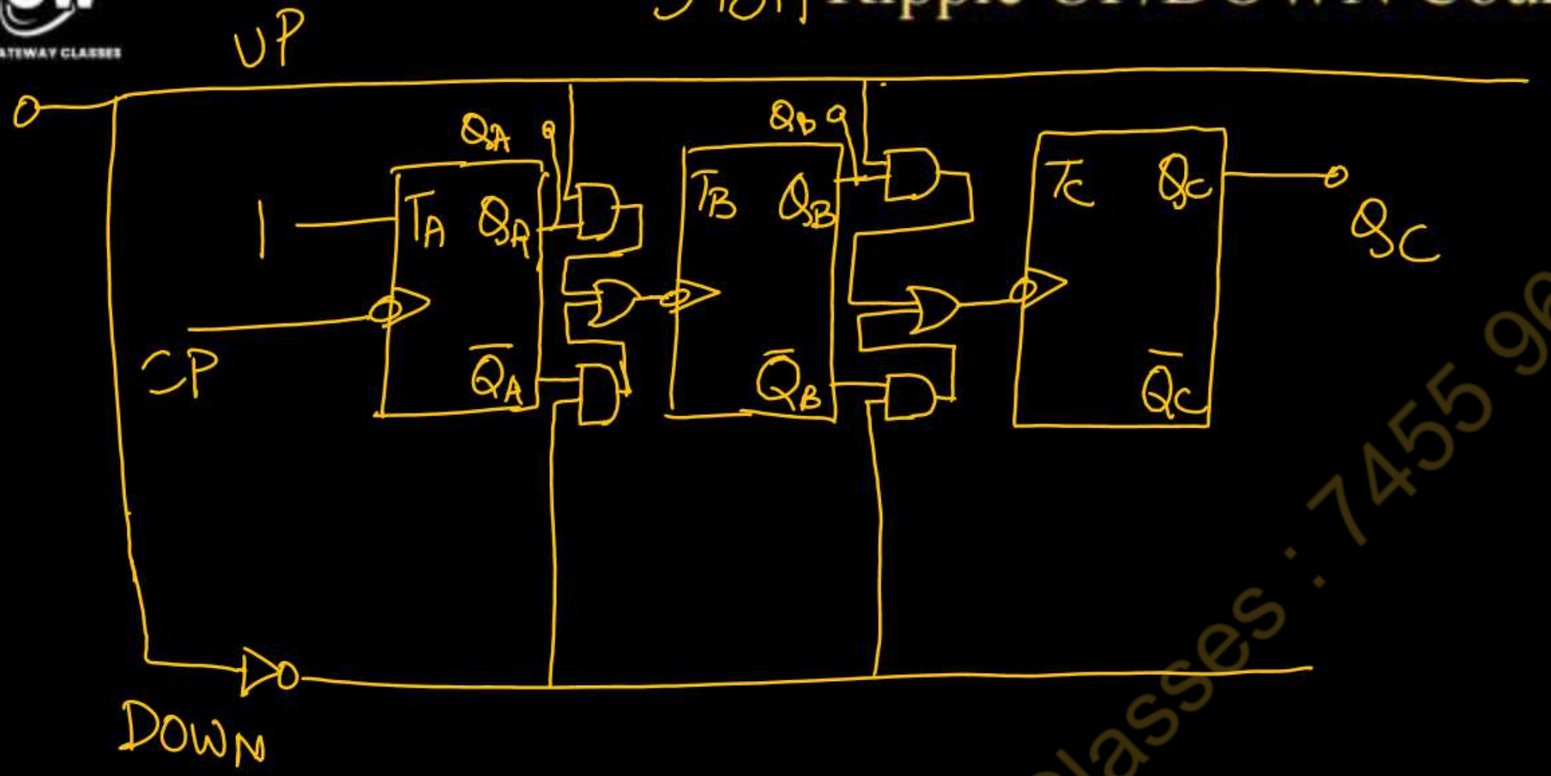
- Ripple UP/DOWN Counter
- Synchronous UP/DOWN Counters
- Excitation Tables & Truth Table of FFs
- MOD COUNTER
- University Questions

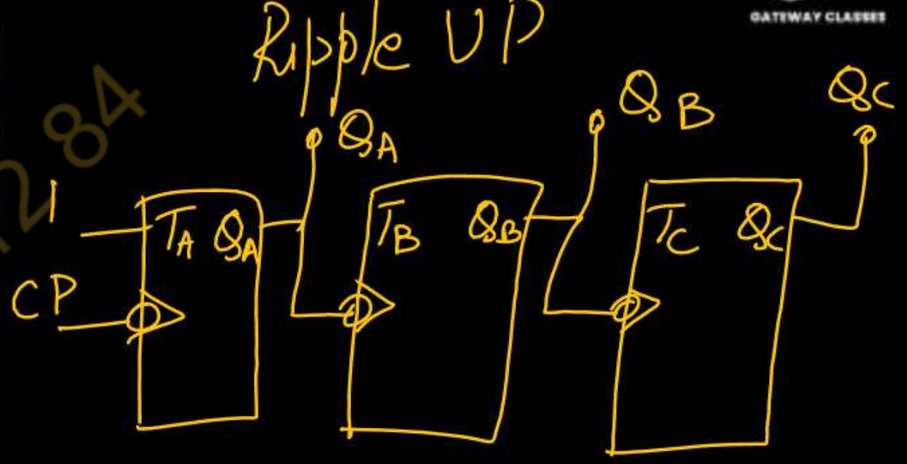
UNIVERSITY QUESTIONS

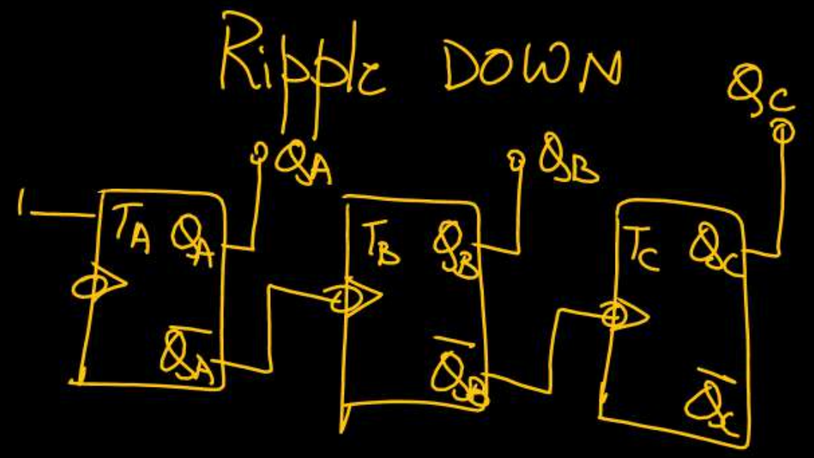
YEAR	QUESTIONS	MARKS
22-23	Design and draw State Diagram for a 2 bit up/down counter	2 Marks
22-23	Design a 3 bit up/down ripple counter	10 Marks
21-22	Design a mod 11 up ripple counter using T-FF	10 Marks
20-21	Design and implement a synchronous 3-bit up/down counter using JK flip-flops.	10 Marks
18-19	What is modulus of a counter?	2 Marks
18-19	Design a modulo-4 UP/DOWN counter using JK flip. flop. Design a ripple decade counter using JK flip	7 Marks

Gateway Classes : 7405 9612 84

3 Bit Ripple UP/DOWN Counter

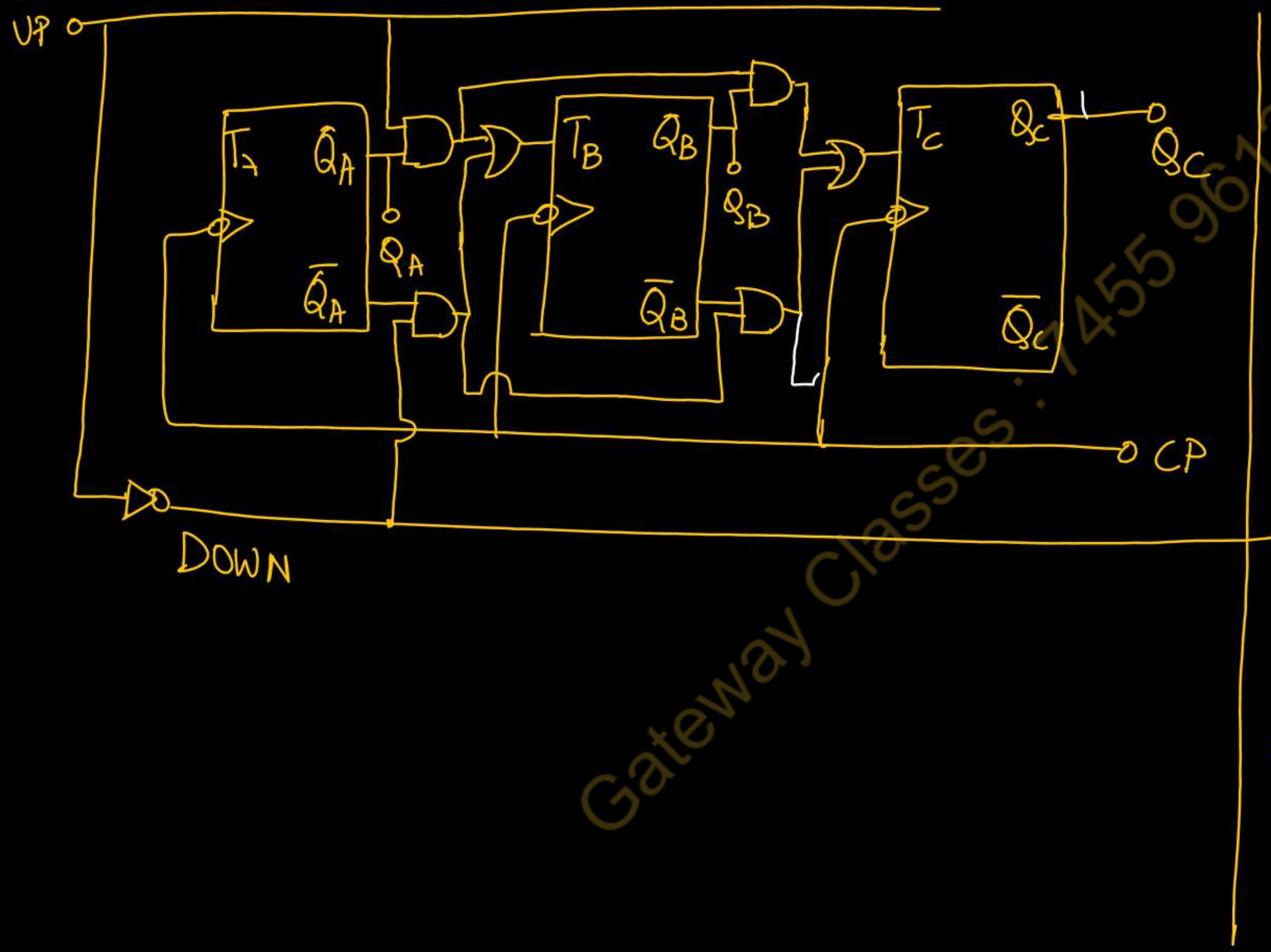




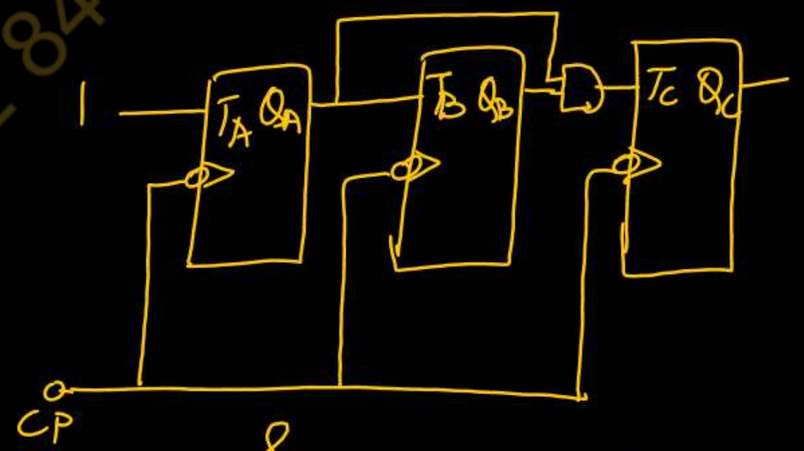


Gateway Classes : 7455 961284

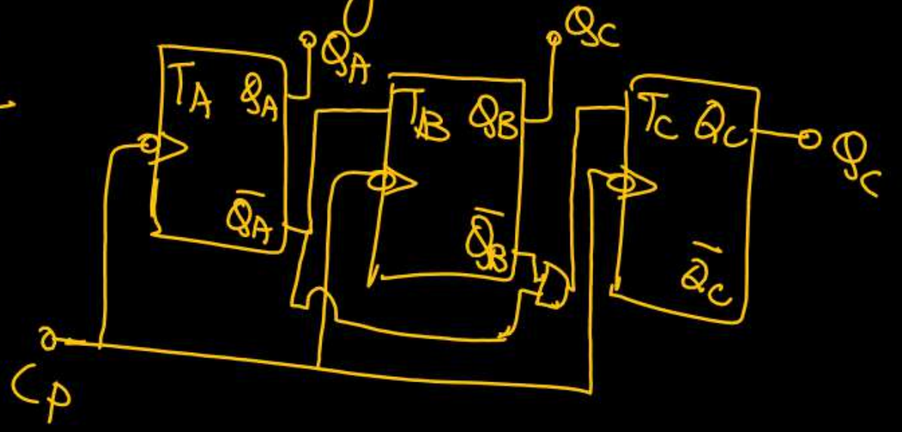
3 bit Synchronous UP/DOWN Counters



Sync. UP



Sync DOWN



Gateway Classes : 7455 9612 84

Excitation Tables & Truth Table of FFs

SR FF Truth Table

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	X

SR FF Excitation Table

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

JK FF Truth Table

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

JK FF Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

D FF Truth Table

D	Q_{n+1}
0	0
1	1

D FF Excitation Table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

T FF Truth Table

T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$

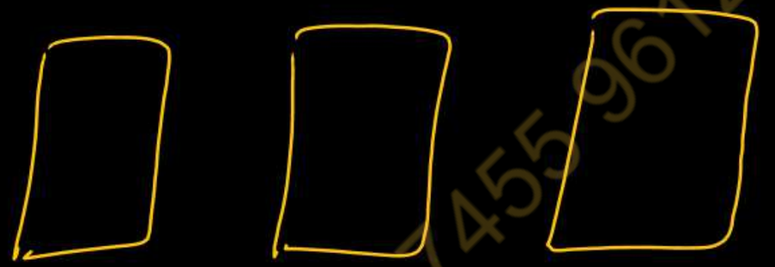
T FF Excitation Table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Gateway Classes : 7455961294

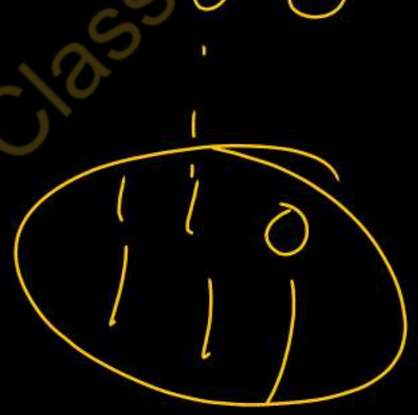
MOD COUNTER

MODULUS COUNTER



MOD 4

0 1 2 3



MOD 5 → 101

0 1 2 3 4

MOD 11 → 1011

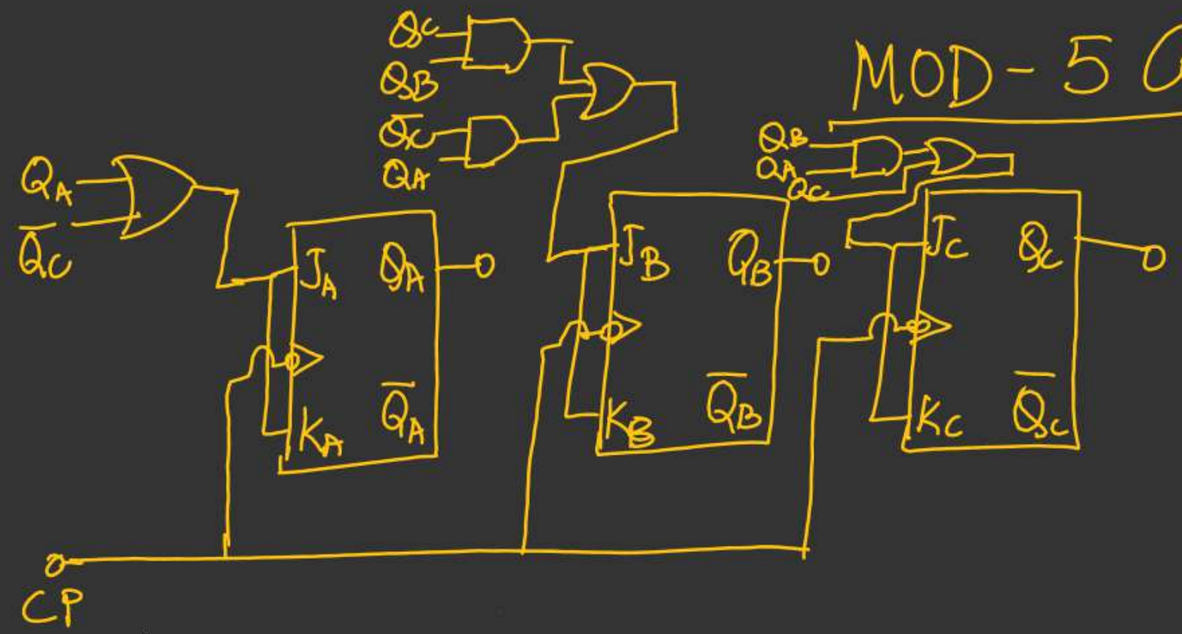
0 - - - - 10

DECADE

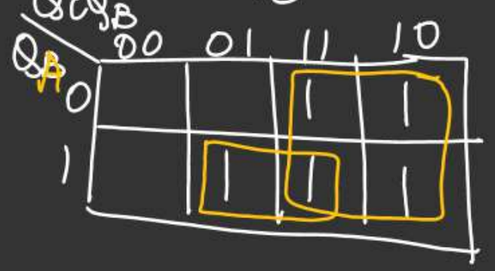
0 - - - 9 → 1010

Gateway Classes : 7455 9612 84

MOD - 5 Counter

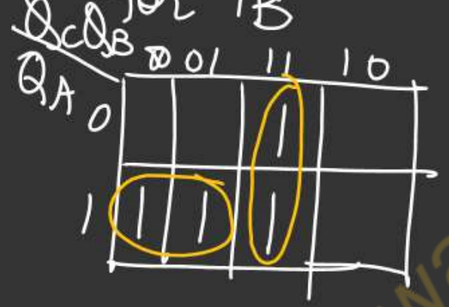


for T_C



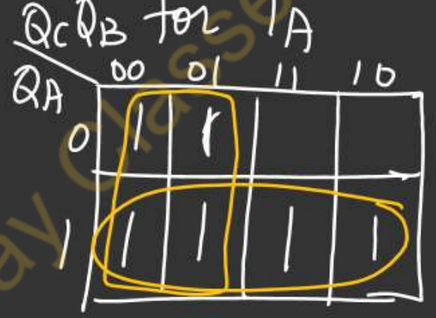
$$T_C = Q_C + Q_B Q_A$$

for T_B



$$T_B = Q_C Q_B + \bar{Q}_C Q_A$$

for T_A



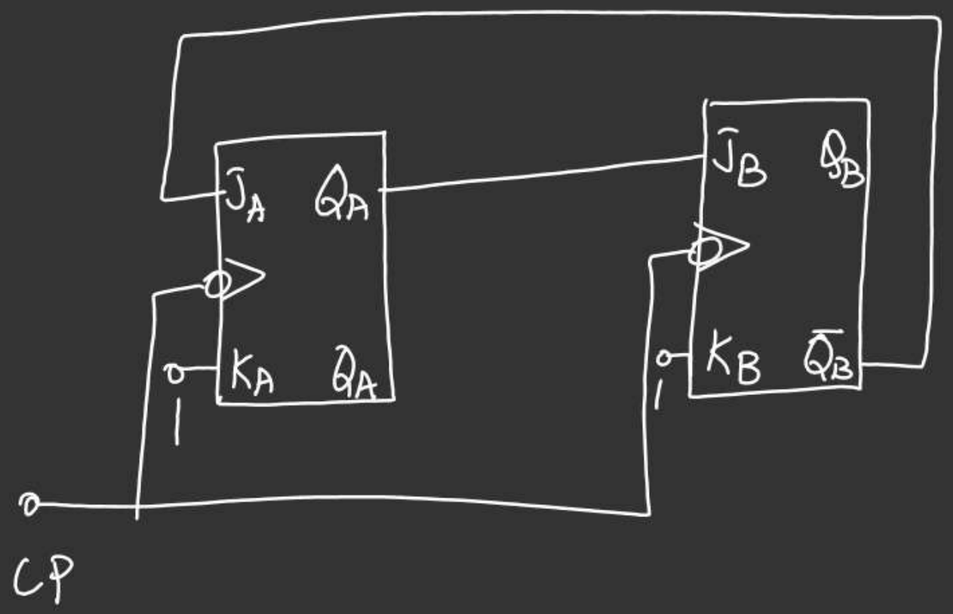
$$T_A = Q_A + \bar{Q}_C$$

State Table

Present state			Next state					
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	T_C	T_B	T_A
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	0	0	0	1	0	0
1	0	1	0	0	0	1	0	1
1	1	0	0	0	0	1	1	0
1	1	1	0	0	0	1	1	1

Gateway Classes : 7455 3612 54

MOD-3 Counter using JK-FF

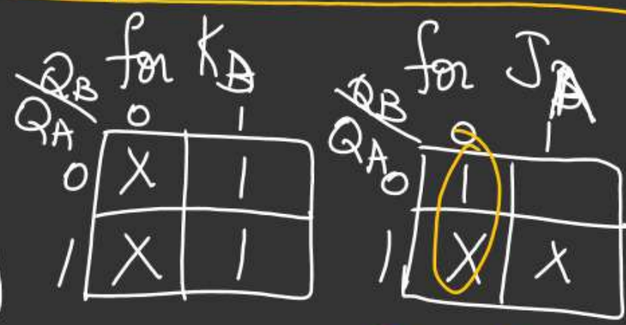


State Table

Present State		Next State		I/Ps			
Q_B	Q_A	Q_{B+1}	Q_{A+1}	J_B	K_B	J_A	K_A
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	0	0	X	1	0	X
1	1	0	0	X	1	X	1



$J_A = Q_A$



$K_A = 1$

$J_B = \bar{Q}_A$

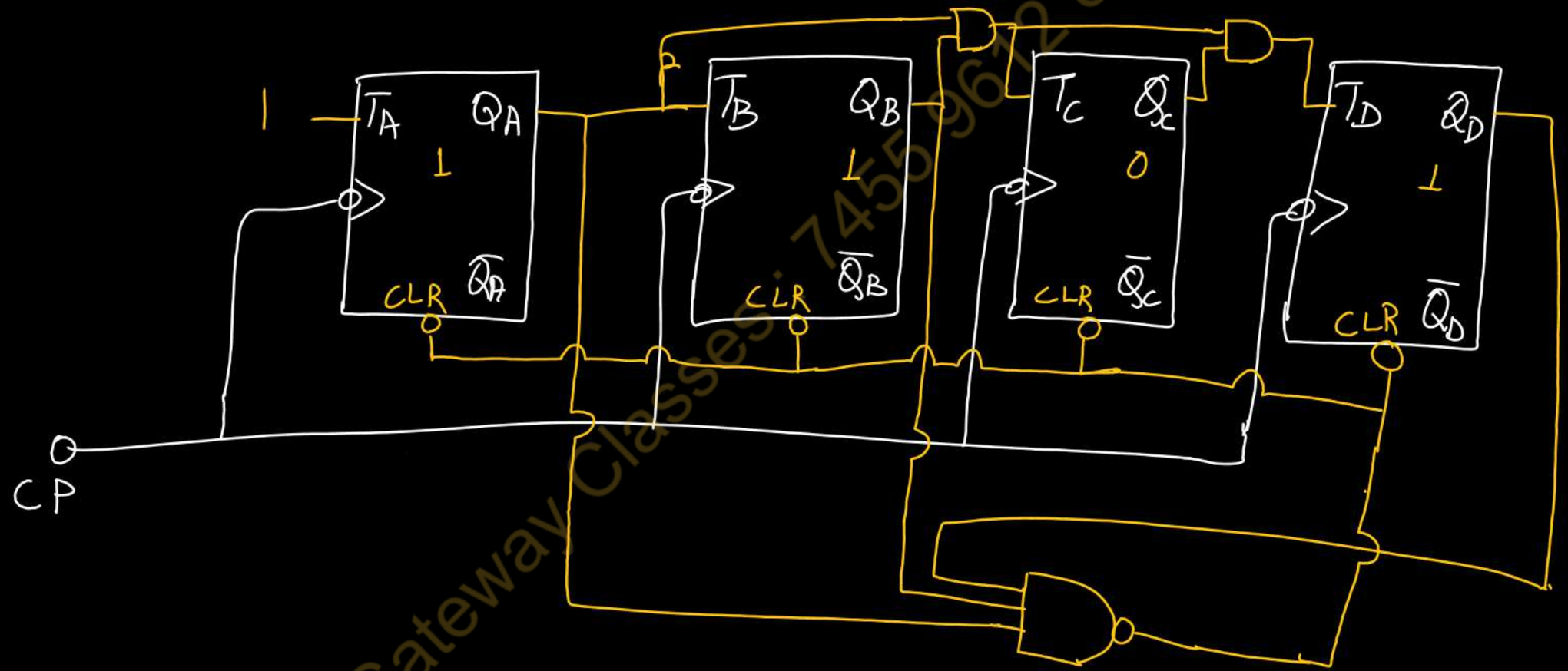


$K_B = 1$

Gateway Classes : 7455 962 84

Other Way of MOD Counter

MOD - 11



Gateway Classes: 7455 96 12 84

DIGITAL SYSTEM DESIGN

UNIT 3 : Sequential logic design

Lec 6

Today's Target

- Specific Sequence Counters
- Ring Counters
- Johnson Counter
- Advantages, Disadvantages & Applications of Johnson counter
- Flip Flop Conversion
- University Questions

Gateway Classes : 7455 961 284

UNIVERSITY QUESTIONS

YEAR	QUESTIONS	MARKS
20-21	Explain 4bit Johnson counter with circuit diagram and waveforms.	10 Marks
18-19	How many flip flops are required to design Mod-5 Ring counter and Mod-5 Johnson counter?	2 Marks

Gateway Classes : 1455 9612 84

Specific Sequence Counters

By using suitable flip flop design a counter to go through the following states:

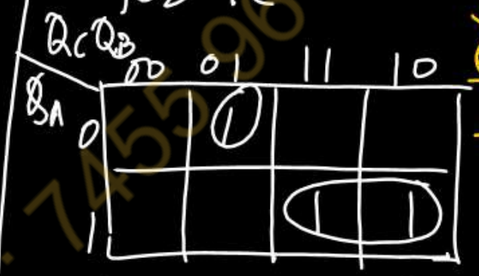


0 → 2 → 4 → 6 → 7 → 0 Avoid Lockout condition.

State Table

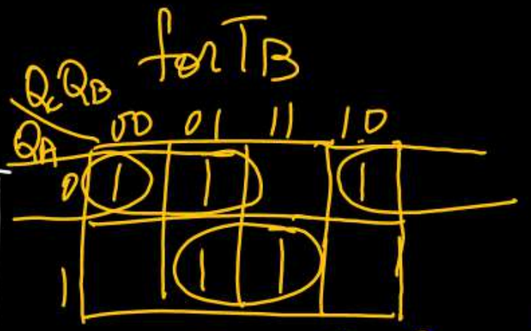
Present state Q_C	Q_B	Q_A	Next state Q_{C+1}	Q_{B+1}	Q_{A+1}	Excitation inputs T_C	T_B	T_A
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	1	0
0	1	1	0	0	0	0	1	1
1	0	0	1	1	0	0	1	0
1	0	1	0	0	0	1	0	1
1	1	0	0	0	1	1	0	1
1	1	1	0	0	0	1	1	1

for T_C



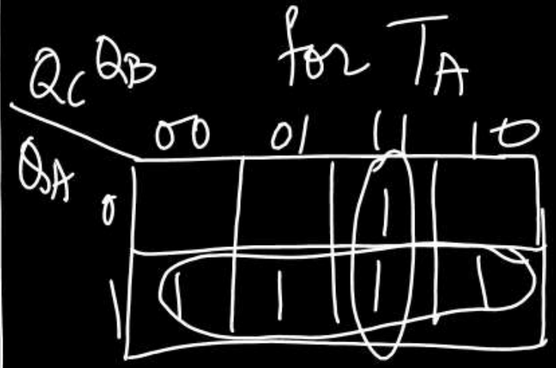
$T_C = Q_C Q_A + \bar{Q}_C Q_B \bar{Q}_A$

for T_B



$T_B = Q_B Q_C + \bar{Q}_C \bar{Q}_A + \bar{Q}_B \bar{Q}_A$

for T_A



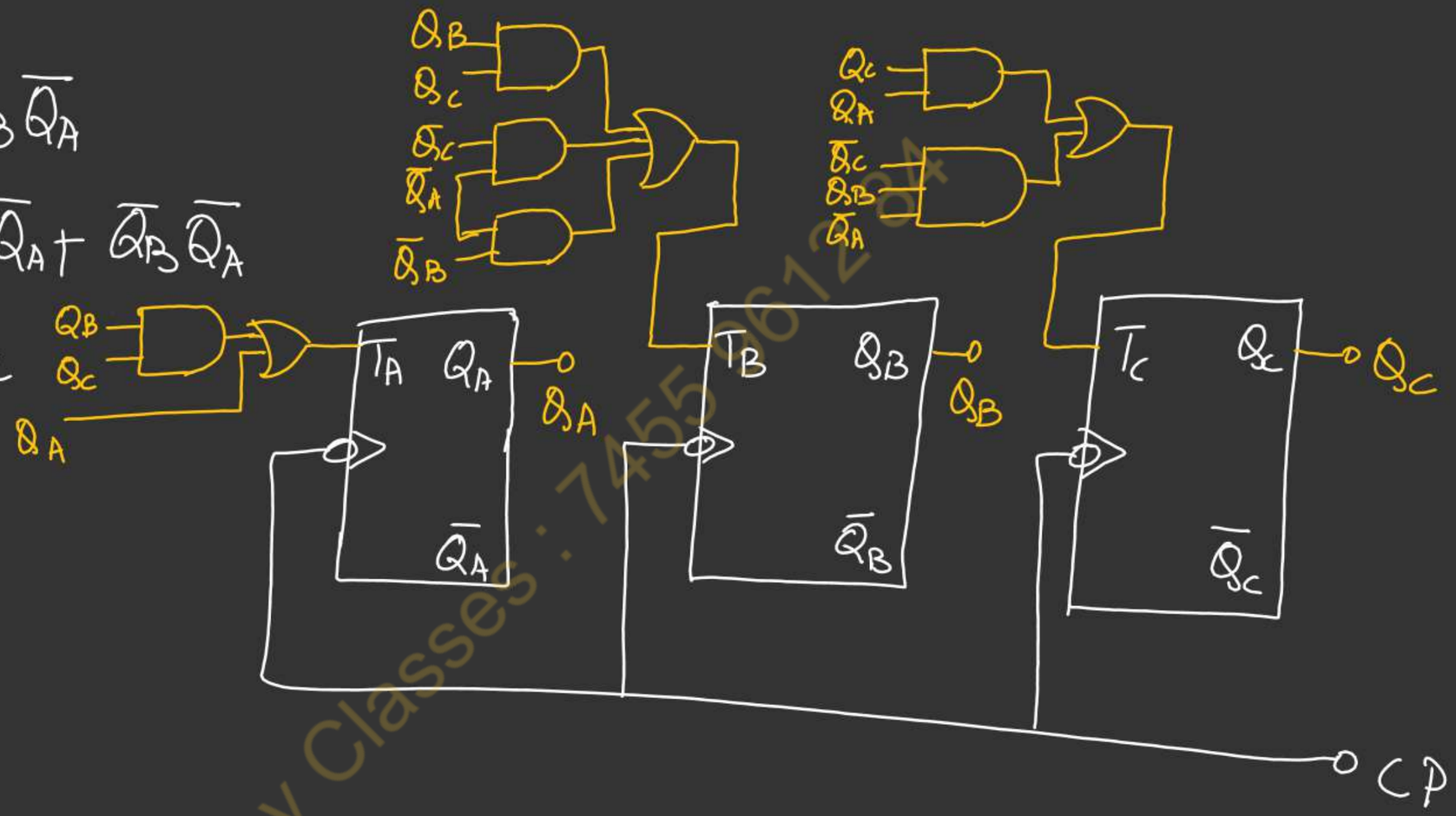
$T_A = Q_A + Q_C Q_B$

Gateway Classes: 7455961284

$$T_C = Q_C Q_A + \bar{Q}_C Q_B \bar{Q}_A$$

$$T_B = Q_B Q_C + \bar{Q}_C \bar{Q}_A + \bar{Q}_B \bar{Q}_A$$

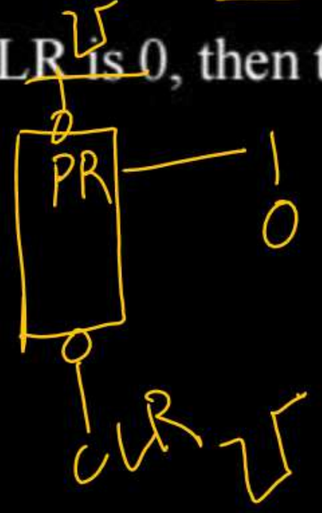
$$T_A = Q_A + Q_B Q_C$$



Gateway Classes : 7455961284

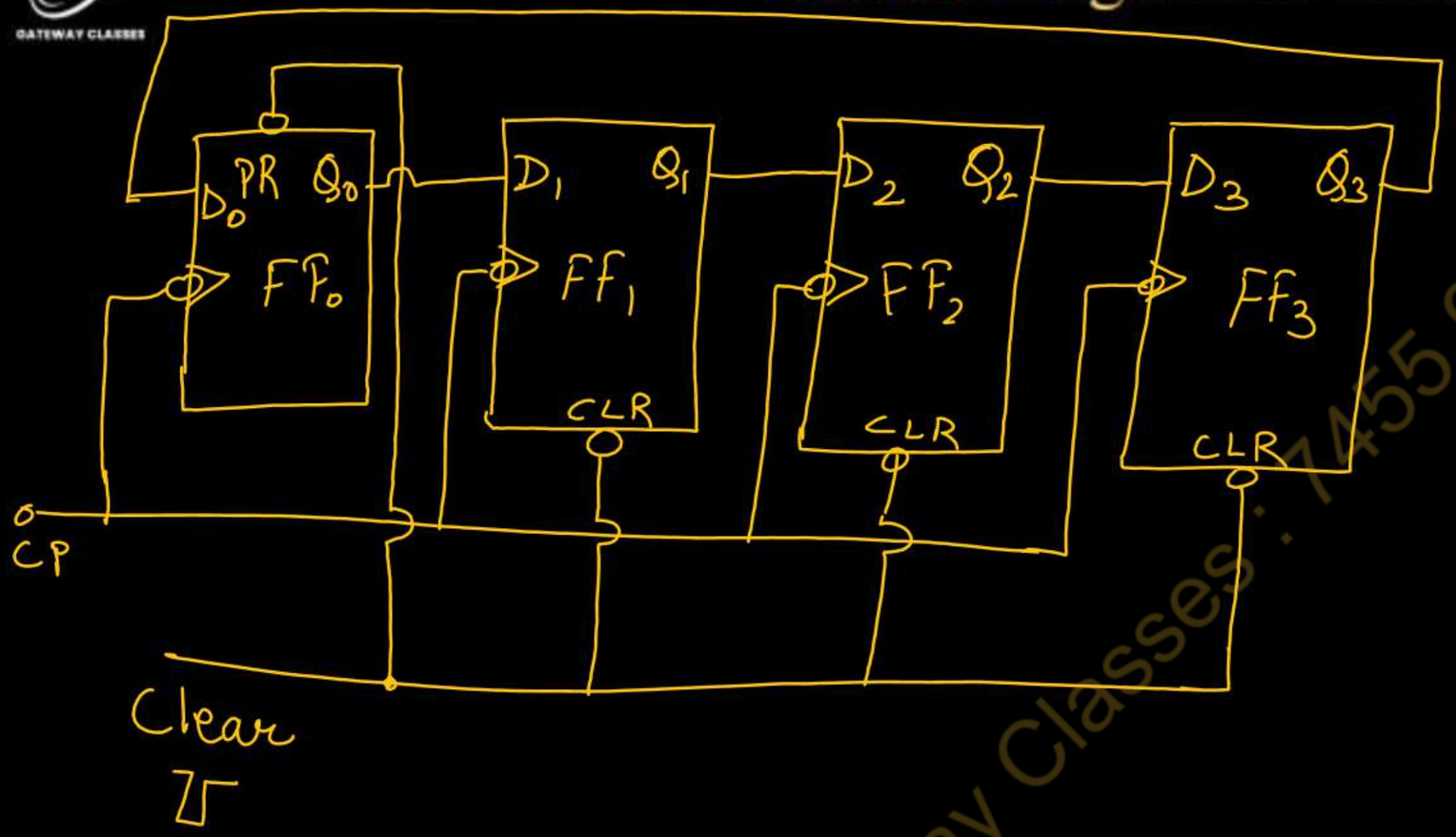
Ring Counters

- A ring counter is a typical application of the Shift register.
- The only change is that the output of the last flip-flop is connected to the input of the first flip-flop in the case of the ring counter but in the case of the shift register it is taken as output.
- No. of states in Ring counter = No. of flip-flop used. So, for designing a 4-bit Ring counter we need 4 flip-flops.
- The clock pulse (CLK) is applied to all the flip-flops simultaneously. Therefore, it is a Synchronous Counter.
- Here we use Overriding input (ORI) for each flip-flop, Preset (PR) and Clear (CLR)
- When PR is 0, then the output is 1. And when CLR is 0, then the output is 0.



Gateway Classes : 7455061284

Circuit Diagram & Truth Table



ORI	CLK	Q0	Q1	Q2	Q3
1/0	X	1	0	0	0
1	↓	0	1	0	0
1	↓	0	0	1	0
1	↓	0	0	0	1
1	↓	1	0	0	0
1					
1					
1					

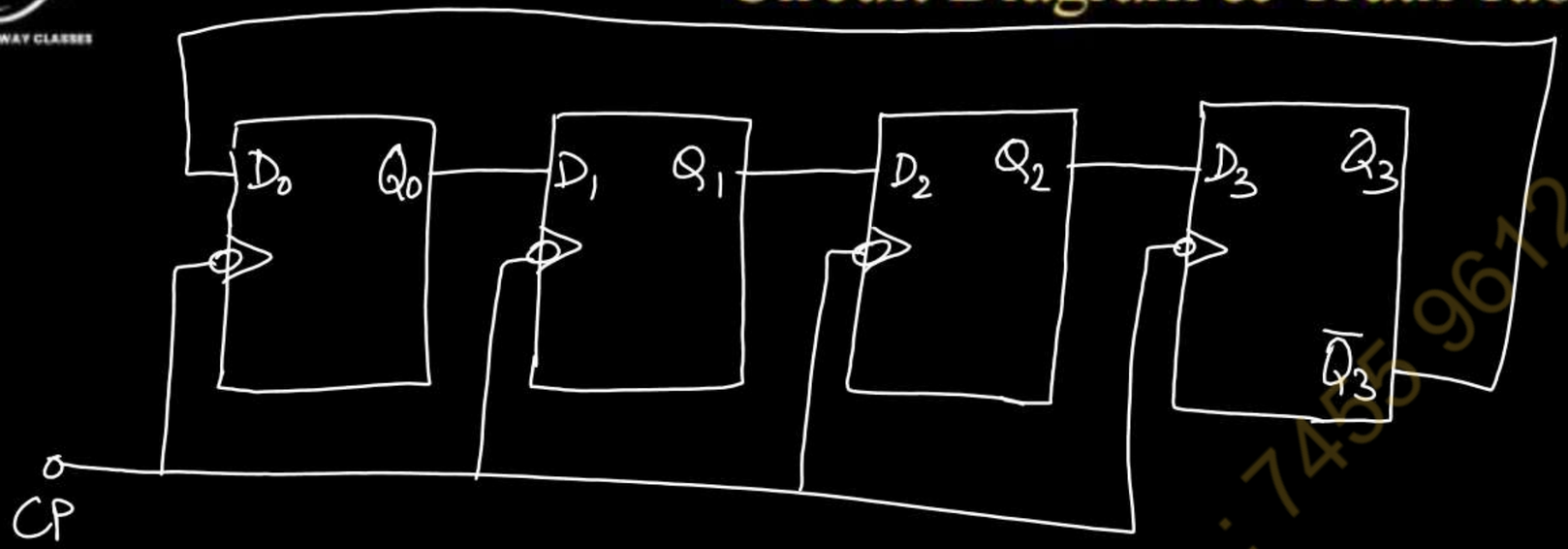
Gateway Classes : 7455 9612 84

Johnson Counter

- Johnson counter also known as creeping counter
- It is an example of synchronous counter.
- In Johnson counter, the complemented output of last flip flop is connected to input of first flip flop
- To implement n-bit Johnson counter we require n flip-flop.
- Another name of Johnson counter are:creeping counter, twisted ring counter, walking counter, mobile counter and switch tail counter.
- Total number of used and unused states in n-bit Johnson counter:
  number of used states=2n
  number of unused states=2n – 2*n

Gateway Classes : 7455 9612 84

Circuit Diagram & Truth Table



	CLK	Q0	Q1	Q2	Q3
1		0	0	0	0
2	↓	1	0	0	0
3	↓	1	1	0	0
4	↓	1	1	1	0
5	↓	1	1	1	1
6	↓	0	1	1	1
7	↓	0	0	1	1
8	↓	0	0	0	1
	↓	0	0	0	0

Gateway Classes : 7455 9612 84

Advantages, Disadvantages & Applications of Johnson counter:

Advantages of Johnson counter:

The Johnson counter has same number of flip flop but it can count twice the number of states the ring counter can count.

- It can be implemented using D and JK flip flop.
- Johnson ring counter is used to count the data in a continuous loop.
- Johnson counter is a self-decoding circuit.

Disadvantages of Johnson counter:

Johnson counter doesn't count in a binary sequence.

- In Johnson counter more number of states remain unutilized than the number of states being utilized.
- The number of flip flops needed is one half the number of timing signals.
- It can be constructed for any number of timing sequence.

Applications of Johnson counter:

Johnson counter is used as a synchronous decade counter or divider circuit.

- It is used in hardware logic design to create complicated Finite states machine. ex: ASIC and FPGA design.
- The 3 stage Johnson counter is used as a 3 phase square wave generator which produces 1200 phase shift.
- It is used to divide the frequency of the clock signal by varying their feedback.

Gateway Classes : 7455 9612 84

Flip Flop Conversion

- The main purpose of the flip flop conversion is to convert type- A flip flop into a desired type-B flip flop using some conversion logic.
- The flip flop conversions are classified into different types that are

SR-FF to JK-FF Conversion

JK-FF to SR-FF Conversion

SR-FF to D-FF Conversion

D-FF to SR-FF Conversion

JK-FF to T-FF Conversion

JK-FF to D-FF Conversion

D-FF to JK-FF Conversion

Gateway Classes : 7455 96 12 84

SR-Flip Flop to JK-Flip Flop Conversion

J	K	Qn	Qn+1	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

for S

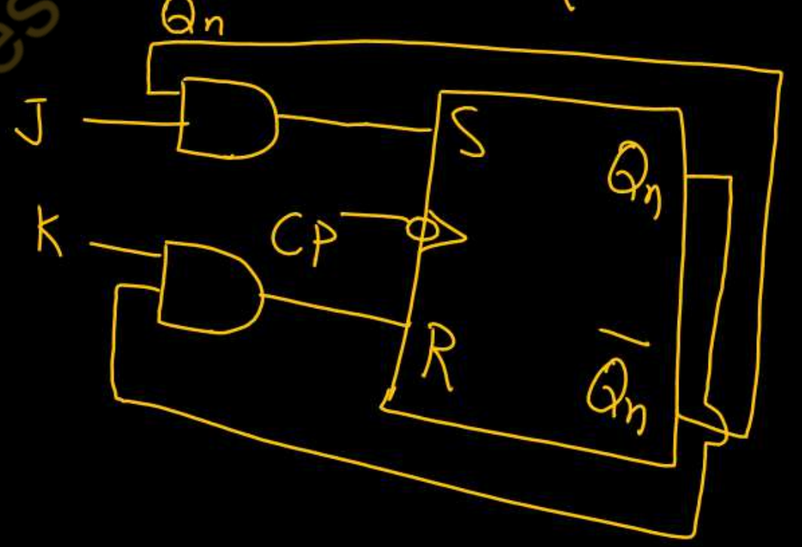
Qn \ JK	00	01	11	10
0			1	1
1	X			X

for R

Qn \ JK	00	01	11	10
0	X	X		
1		1	1	

$S = J\bar{Q}_n$

$R = KQ_n$

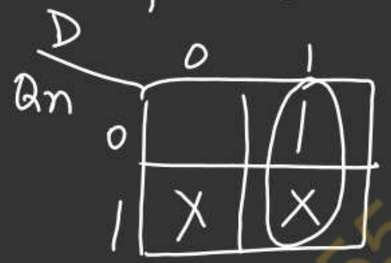


Gateway Classes 7455961284

D FF using JK FF

D	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

for J

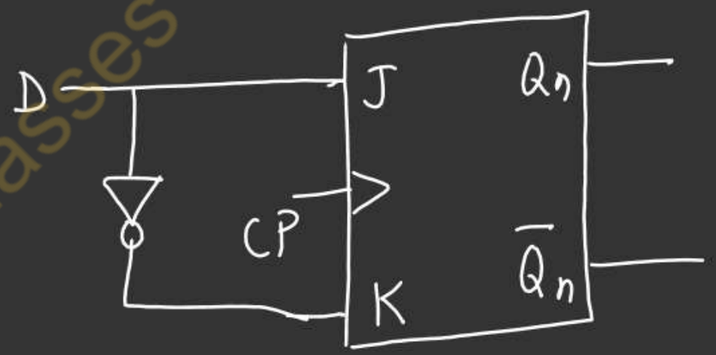


$J = D$

for K



$K = \overline{D}$



Gateway Classes : 7455 96 12 84

DIGITAL SYSTEM DESIGN

UNIT 3 : Sequential logic design

Lec 7

Gateway Classes : 7455 961 284

Today's Target

- Digital Registers
- Serial Input Serial Output
- Serial Input Parallel Output
- Parallel Input Parallel Output
- Parallel Input Serial Output

Digital Registers

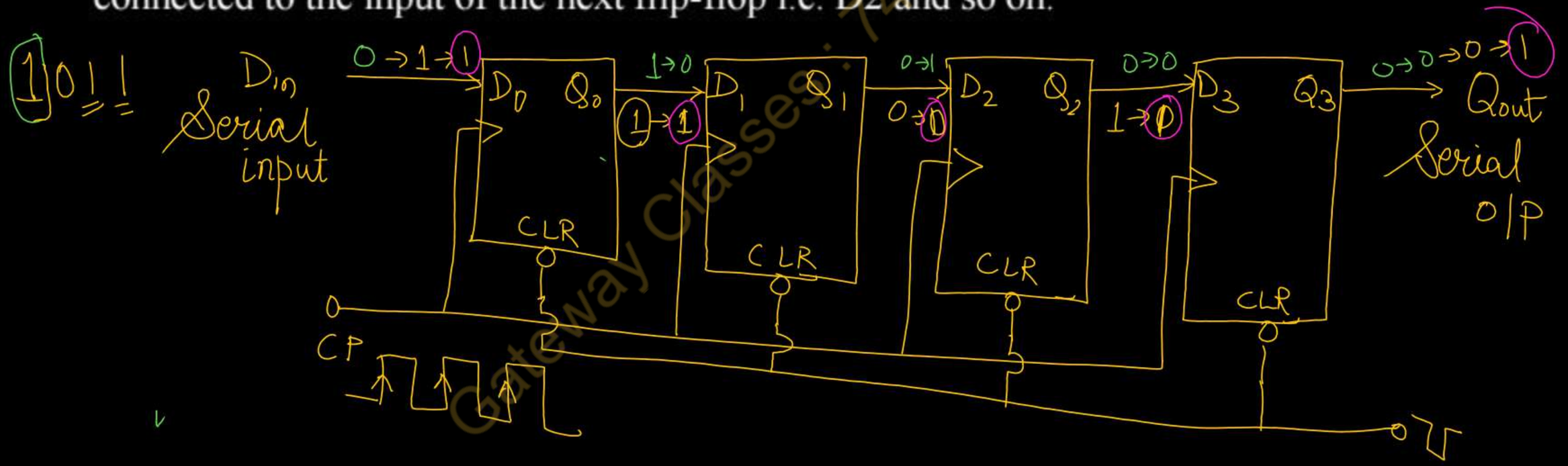
- One flip-flop can store one-bit of information.
- In order to store multiple bits of information, we require multiple flip-flops.
- The group of flip-flops, which are used to hold store the binary data is known as **register**.
- If the register is capable of shifting bits either towards right hand side or towards left hand side is known as shift register.
- An 'N' bit shift register contains 'N' flip-flops.
- Following are the four types of shift registers based on applying inputs and accessing of outputs.
- Serial Input Serial Output — SISO
- Serial Input Parallel Output — SIPO
- Parallel Input Serial Output — PISO
- Parallel Input Parallel Output — PIPO

Gateway Classes : 7455961284

Serial Input Serial Output

SISO

- Let all the flip-flop be initially in the reset condition i.e. Q3 = Q2 = Q1 = Q0 = 0.
- If an entry of a four bit binary number 1 1 1 1 is made into the register, this number should be applied to Din bit with the LSB bit applied first.
- The D input of FF-3 i.e. D3 is connected to serial data input Din. Output of FF-3 i.e. Q3 is connected to the input of the next flip-flop i.e. D2 and so on.

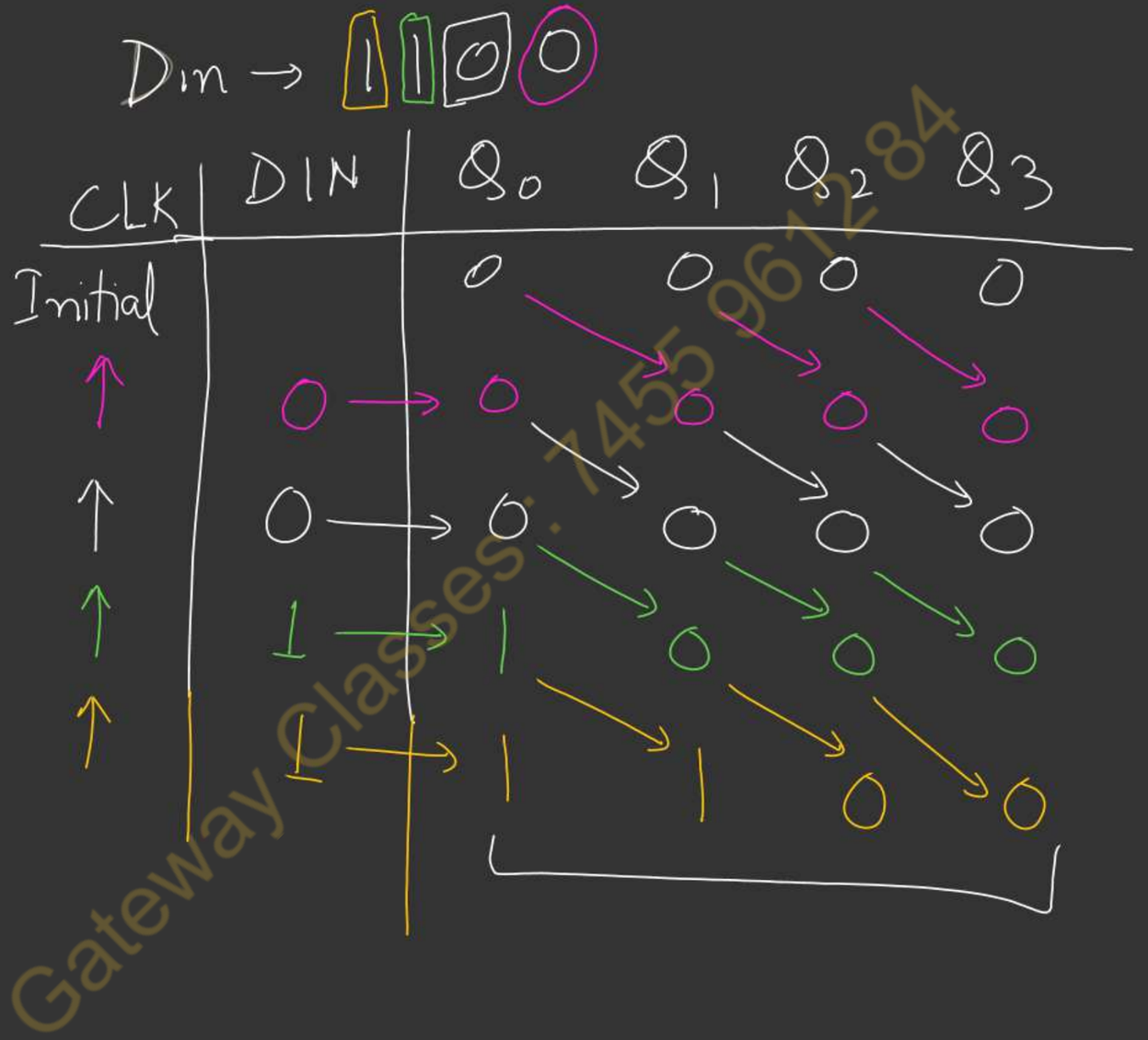


Gateway Classes : 7155 9612 84

Truth Table

CLK	Din	Q3	Q2	Q1	Q0
Initially	1 0 1 1	0	0	0	0
↑	1	1	0	0	0
↑	0	0	1	0	0
↑	1	1	0	1	0
↑	1	1	1	0	1

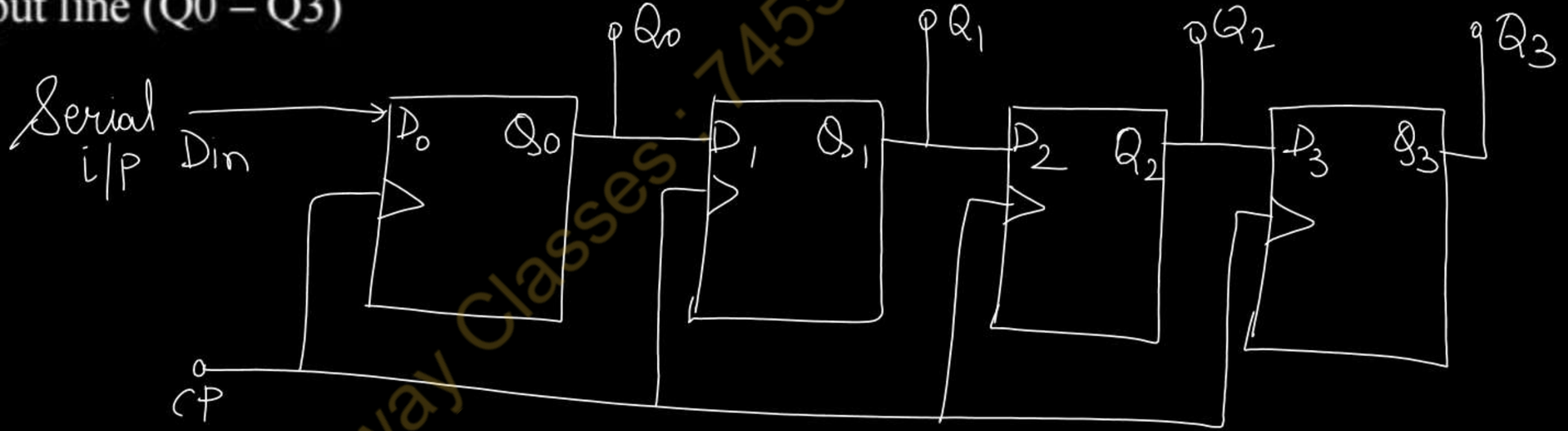
Gateway Classes : 7455962284



Gateway Classes: 7455 961284

Serial in – Parallel out Shift Register

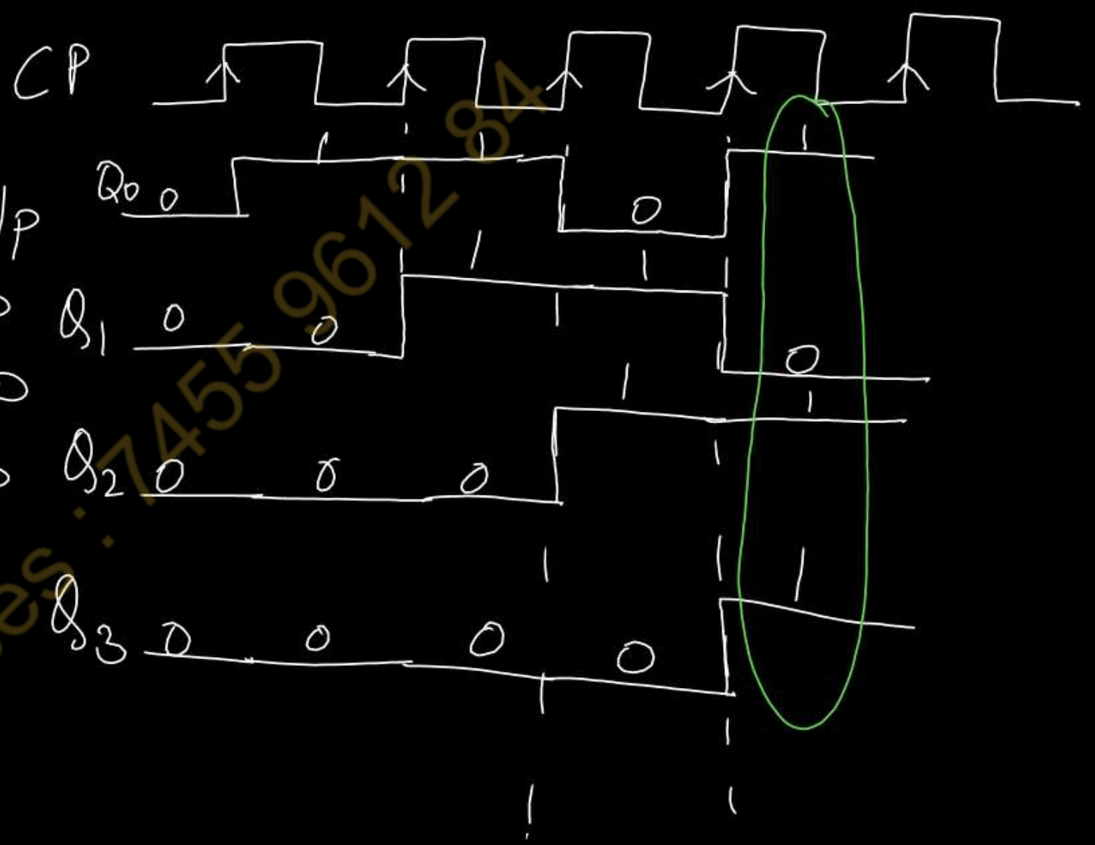
- used for the conversion of data from serial to parallel.
- The data comes in one after the other per clock cycle and can either be shifted and replaced or be read off at each output.
- This means when the data is read in, each read in bit becomes available simultaneously on their respective output line (Q0 – Q3)



Gateway Classes : 7455961284

Truth Table & Waveforms

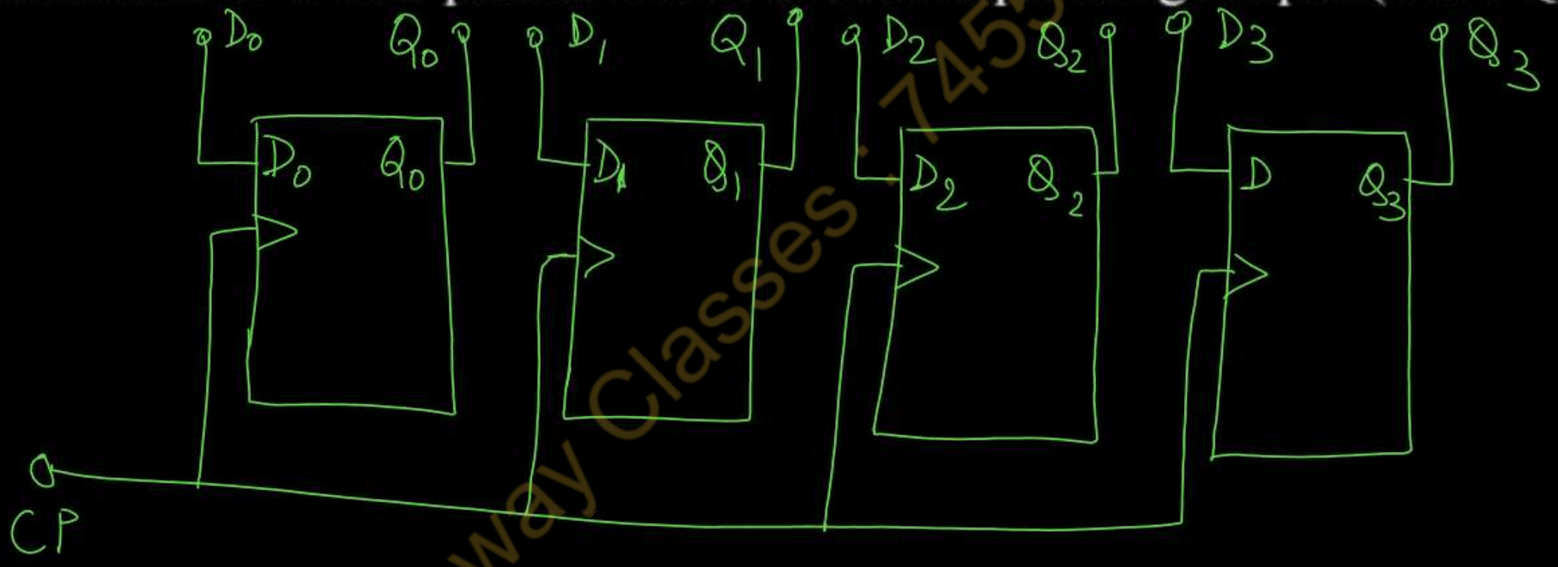
	FF0	FF1	FF2	FF3	
CLEAR	0	0	0	0	← CLK 1 O/P
1011	1	0	0	0	← CLK 2 O/P
	1	1	0	0	← CLK 3 O/P
	0	1	1	0	← CLK 4 O/P
	1	0	1	1	



Gateway Classes : 7455 961284

Parallel in – Parallel out shift register

- The output data across the parallel outputs appear simultaneously as the input data is fed in.
- The input data at each of the input pins from D0 to D3 are read in at the same time when the device is clocked and at the same time and passed out at the corresponding output (from Q0 to Q3).

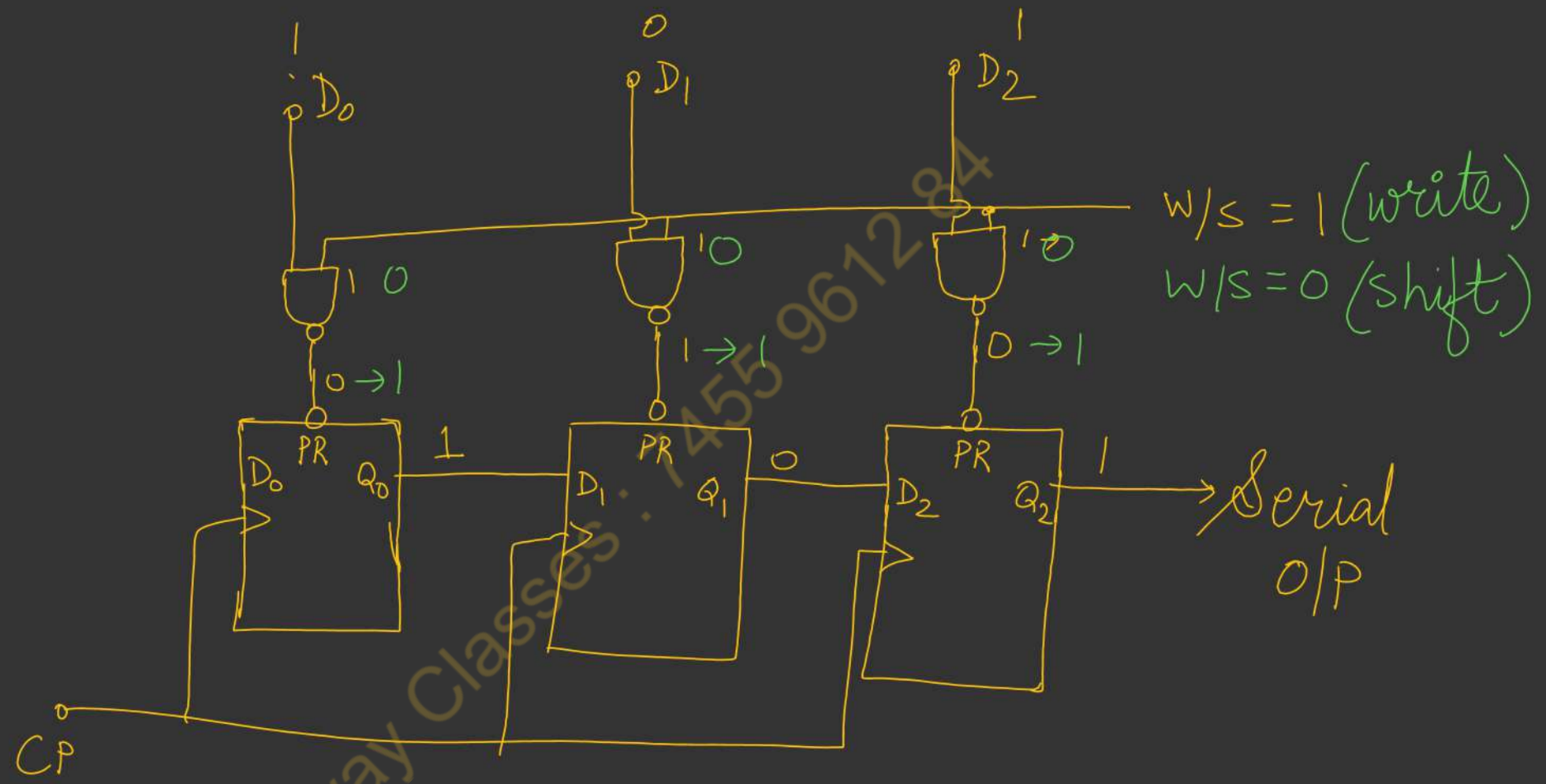


Gateway Classes : 7453 901284

Parallel in – Serial out Shift Register

- The data is supplied in parallel.
- This register can be used to store and shift a 4-bit word, with the write/shift (W/S) control input controlling the mode of operation of the shift register.
- When the W/S =1 (Write Mode), data can be written and clocked in via D0 to D3.
- When W/S =0 (Shift mode), the register then shifts the data out serially on clock input.

Gateway Classes : 7455 961284



Gateway Classes : 7455 961284

DIGITAL SYSTEM DESIGN

UNIT 3 : Sequential logic design

Lec 8

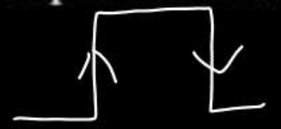
Today's Target

- Finite State Machines
- Mealy State Machine
- Moore State Machine
- Numerical
- University Questions

Gateway Classes : 7455 961 2 84

Finite State Machines

- We know that synchronous sequential circuits change or affect their states for every positive or negative transition of the clock signal based on the input.
- This behavior of synchronous sequential circuits can be represented in the graphical form and it is known as state diagram.



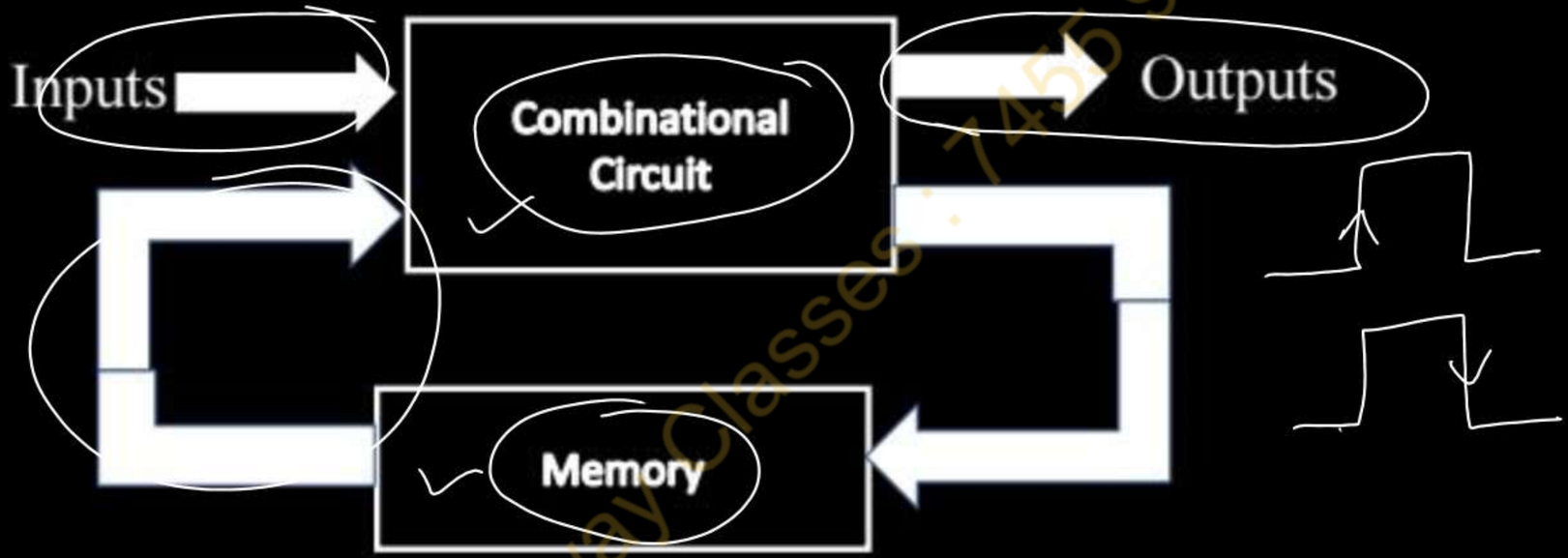
- A synchronous sequential circuit is also called as Finite State Machine FSM, if it has finite number of states.
- There are two types of FSMs.

  1) Mealy State Machine
  2) Moore State Machine

Gateway Classes : 7455 96 42 04

Mealy State Machine

- A Finite State Machine is said to be Mealy state machine, if outputs depend on both present inputs & present states.
- The block diagram of Mealy state machine is shown in the following figure:

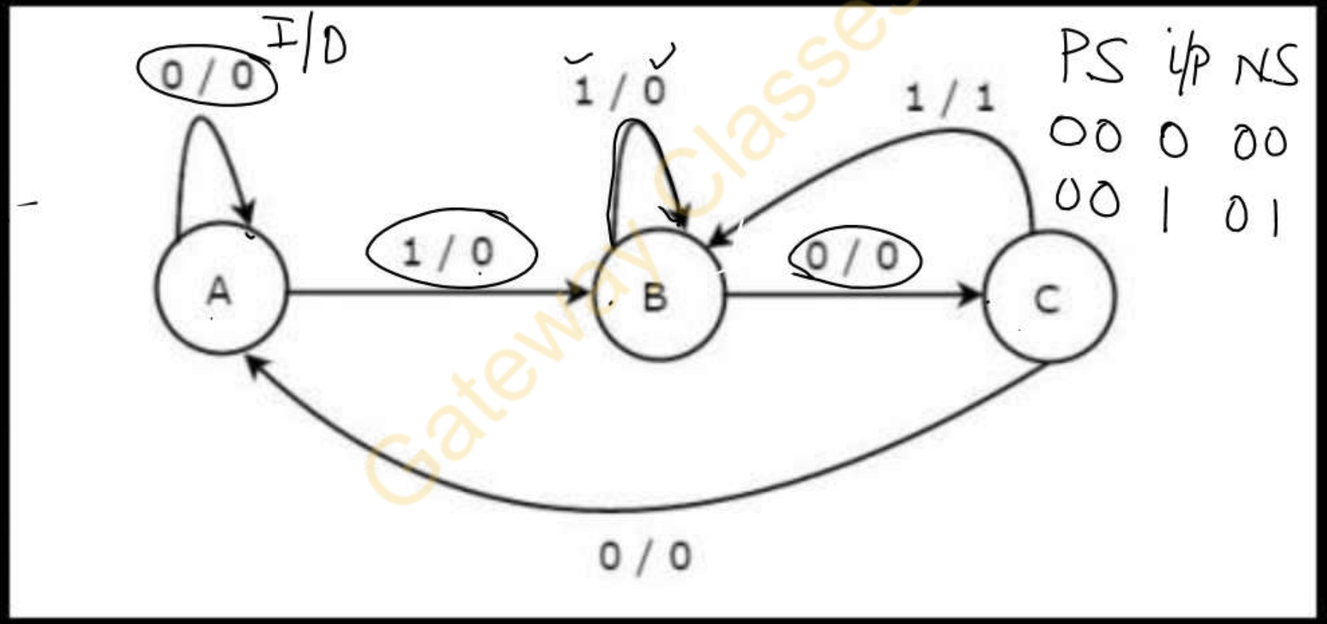


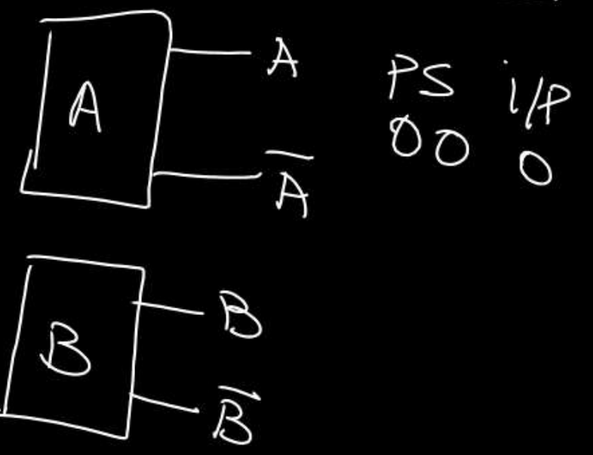
- two parts present in Mealy state machine: combinational logic and memory
- the outputs will be valid only at positive or negative transition of the clock signal.

Gateway Classes : 7455961284

State Diagram of Mealy state machine

- Suppose, there are three states, namely A, B & C.
- These states are labelled inside the circles & each circle corresponds to one state.
- Transitions between these states are represented with directed lines.
- Here, 0 / 0, 1 / 0 & 1 / 1 denotes input / output.
- In the figure, there are two transitions from each state based on the value of input (x).
- In general, the number of states required in Mealy state machine is less than or equal to the number of states required in Moore state machine.

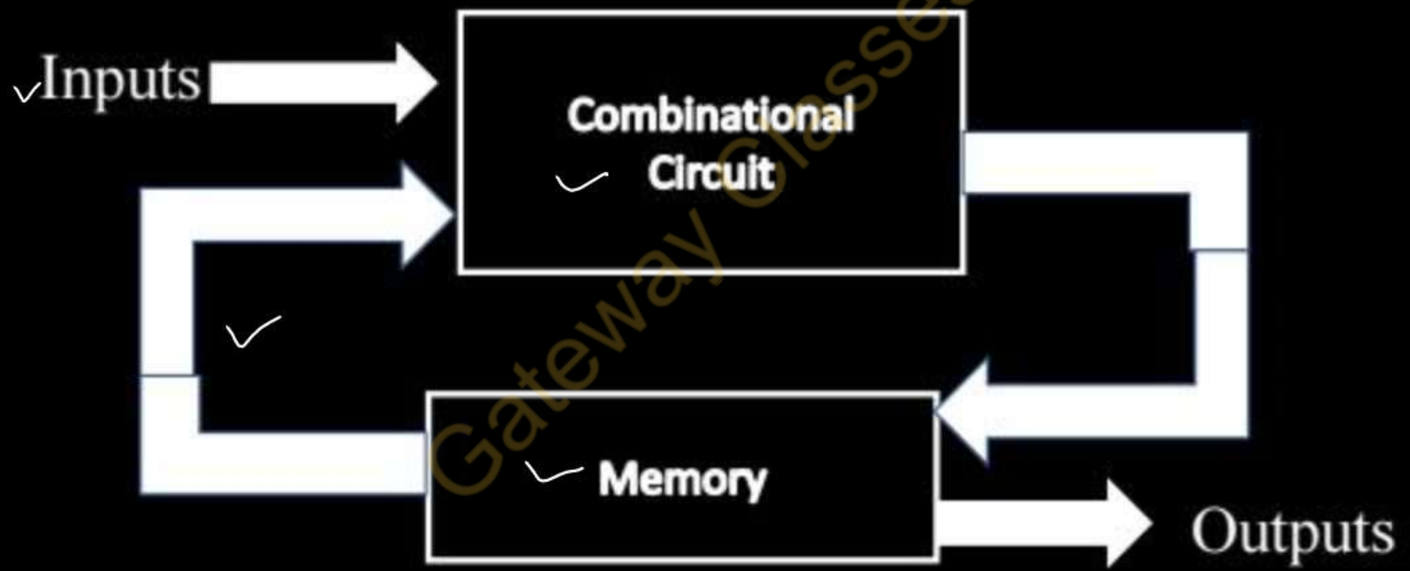




Gateway Classes (455 96 2 84

Moore State Machine

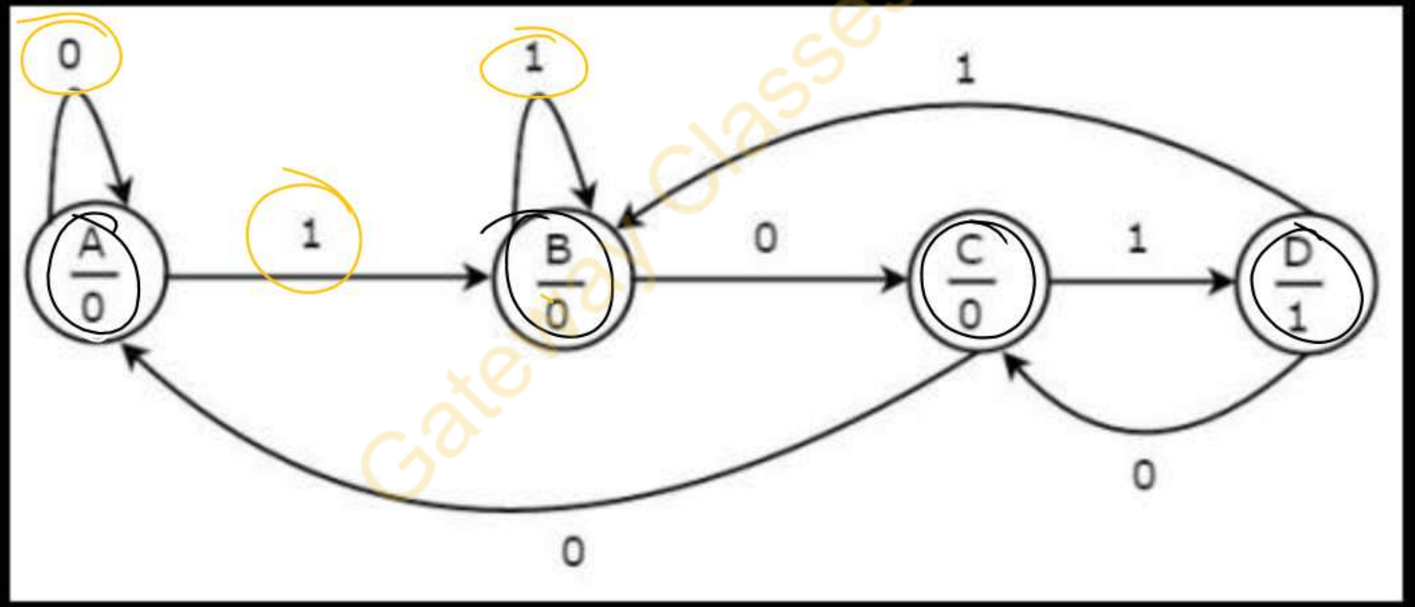
- A Finite State Machine is said to be Moore state machine, if outputs depend only on present states.
- two parts present in Moore state machine: combinational logic and memory.
- the present inputs and present states determine the next states.
- the outputs will be valid only after transition of the state.
- The block diagram of Moore state machine is shown in the following figure.



Gateway Classes : 7455 96 12 84

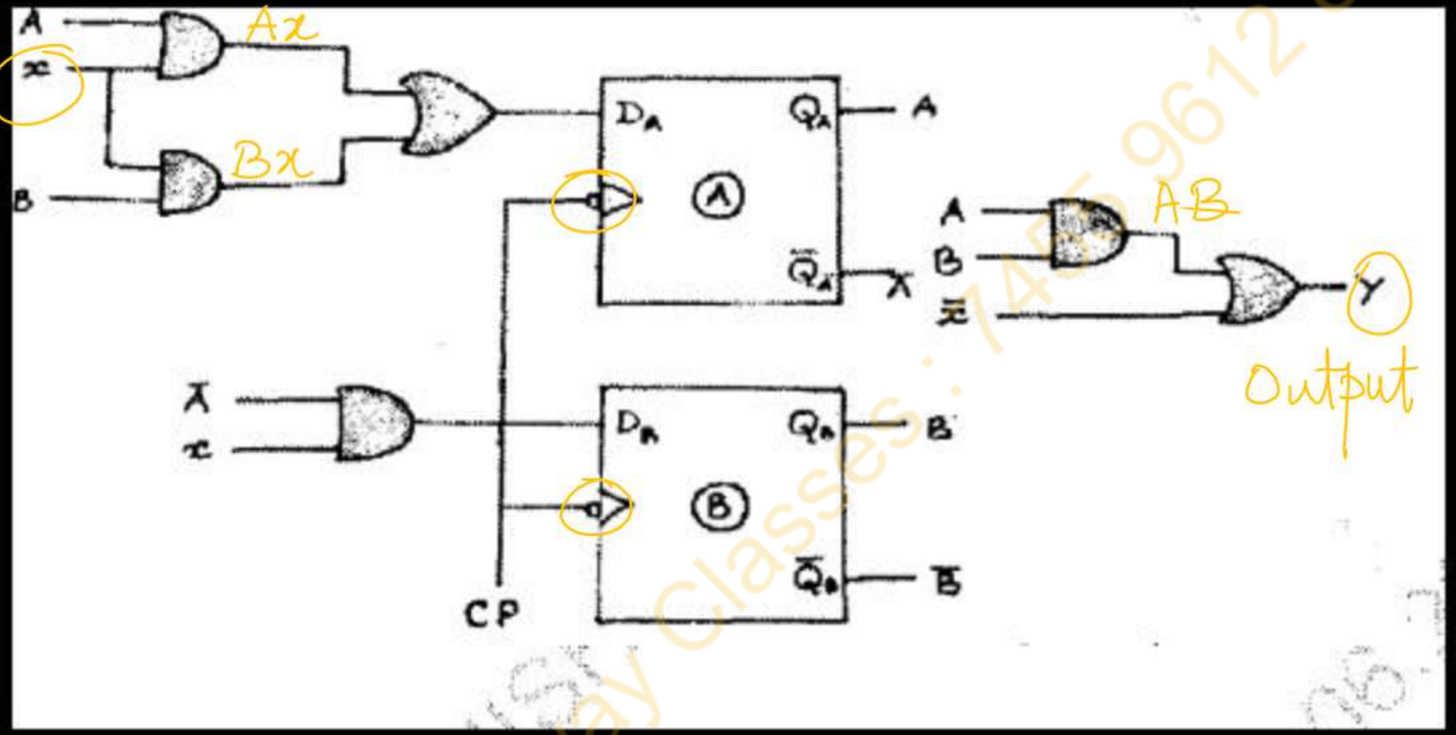
State Diagram of Moore state machine

- Suppose, there are four states, namely A, B, C & D.
- These states and the respective outputs are labelled inside the circles.
- Here, only the input value is labeled on each transition.
- In the figure, there are two transitions from each state based on the value of input, x.
- In general, the number of states required in Moore state machine is more than or equal to the number of states required in Mealy state machine.



Gateway Classes : 7455961284

Derive the state table and state diagram for the Sequential circuit shown in fig, (18-19)



State Equations

$D_A = Ax + B\bar{x} = A$

$D_B = \bar{A}x = B$

$Y = AB + \bar{x}$

Gateway Classes: 7405 9612 84

$$A_{n+1} = Ax + Bx$$

$$B_{n+1} = \bar{A}x$$

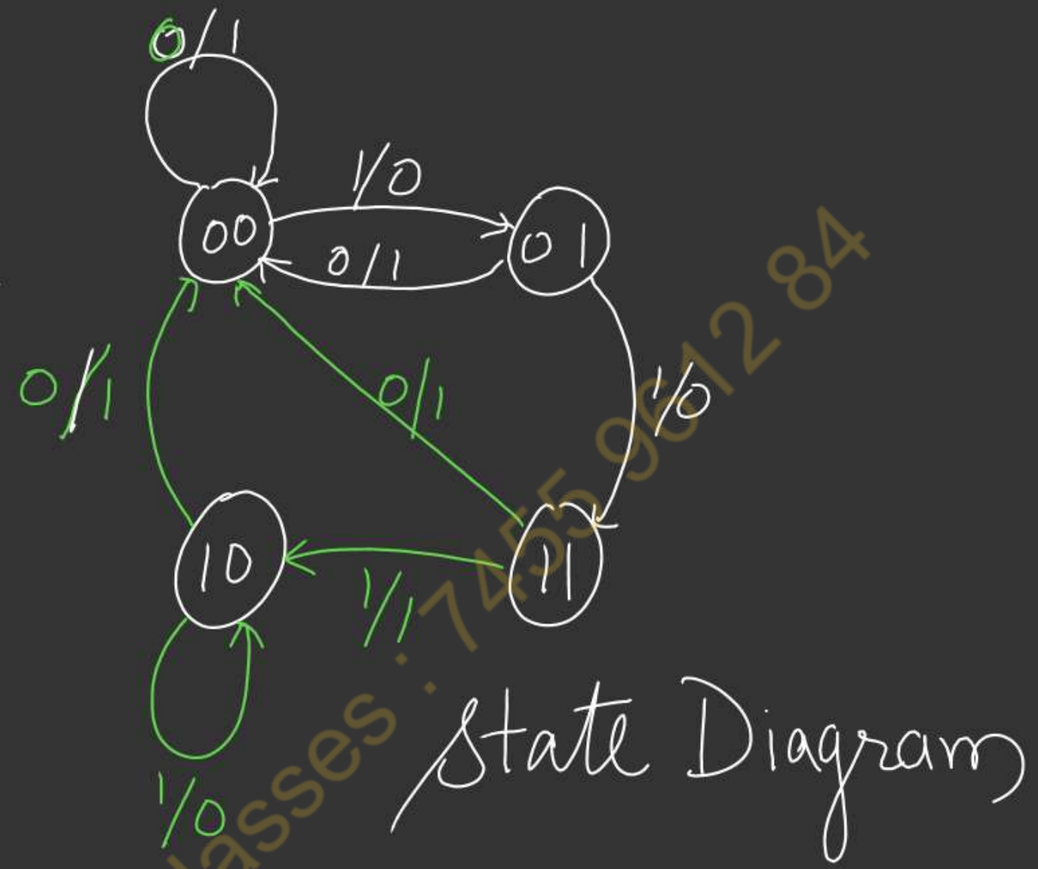
$$y = AB + \bar{x}$$

State Table

Present state		Input	Next State		output
A	B	x	A_{n+1}	B_{n+1}	Y
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	D	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	1

Gateway Classes : 7455 9612 8

A	B	X	A_{n+1}	B_{n+1}	Y
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	1



State Diagram

Gateway Classes : 7455 9612 84

University Questions

Year	Questions	Marks
21-22	Draw and explain block diagram of Moore model and Mealy model.	5 Marks
20-21	For the clocked JK flip-flop write the state table, draw the state diagram and the state equation.	10 Marks
20-21, 19-20	Discuss Mealy and Moore FSM. What do you mean by excitation table?	10 Marks

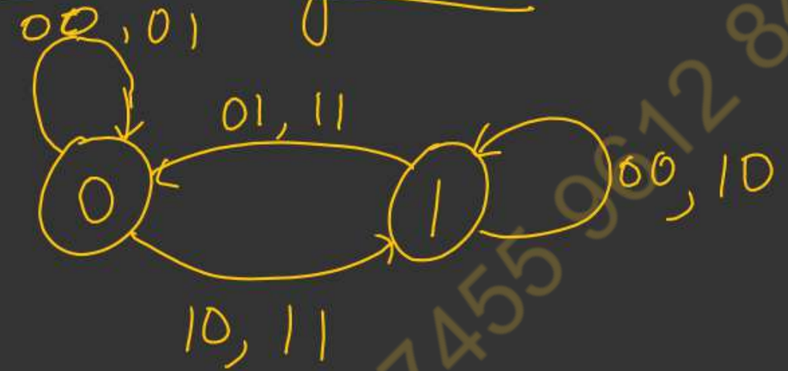
Gateway Classes 7455 9612 84

Clocked JK-FF

J	K	Q	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

State Table

State Diagram



For Q_{n+1}

Q_n \ JK	00	01	11	10
0	0	0	1	1
1	1	0	0	1

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

Gateway Classes: 7455 9612 84

DIGITAL SYSTEM DESIGN

UNIT 3 : Sequential logic design

Lec 9

Gateway Classes : 7455 961284

Today's Target

- Numerical on Sequential Circuit
- Numerical on State Diagram
- Numerical on Asynchronous Circuit

Design a sequential circuit with two Flip Flops, A & B and one input x. When x=0, the State of the circuit remains the same when x=1 the circuit passes through the state transitions from 00 to 01 to 11 to 10 back to 00 & repeat. (22-23, 20-21,19-20)

State Table

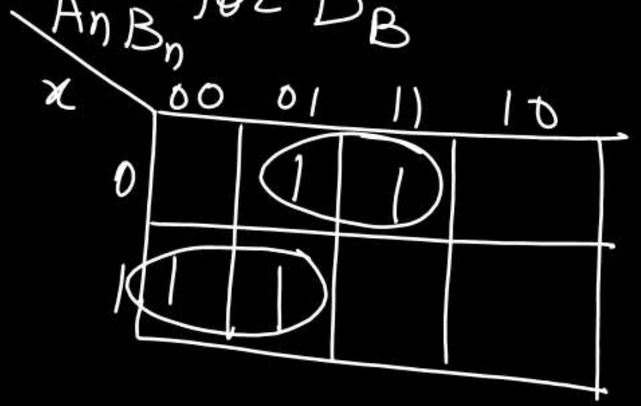
Previous state A_n	Previous state B_n	I/P x	Next state A_{n+1}	Next state B_{n+1}	D_A	D_B
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	0	1	0	1
0	1	1	1	1	1	1
1	0	0	1	0	1	0
1	0	1	0	0	0	0
1	1	0	1	1	1	1
1	1	1	1	0	1	0

for D_A



$D_A = A_n \bar{x} + B_n x$

for D_B

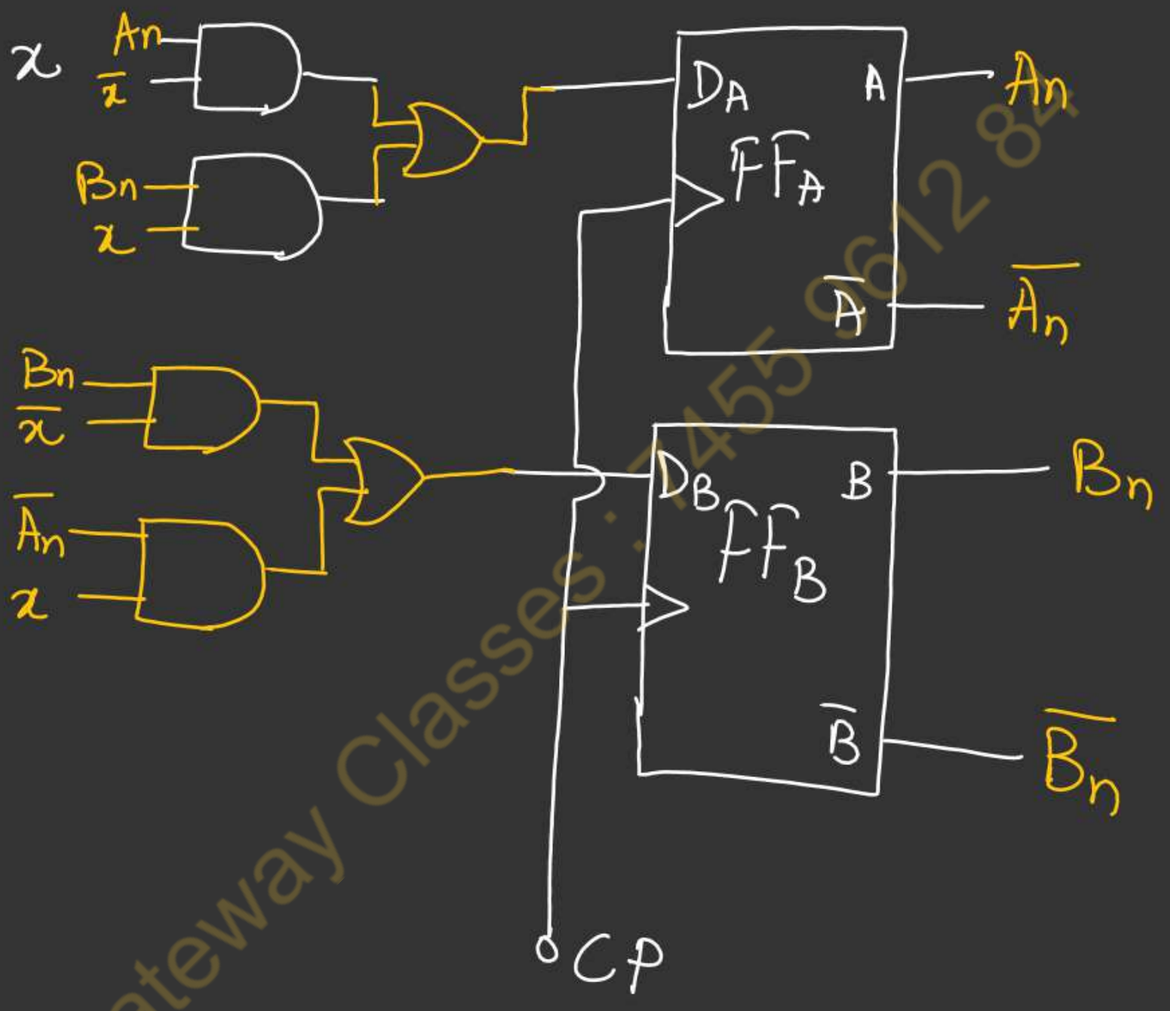


$D_B = B_n \bar{x} + \bar{A}_n x$

Gateway Classes : 7455 961284

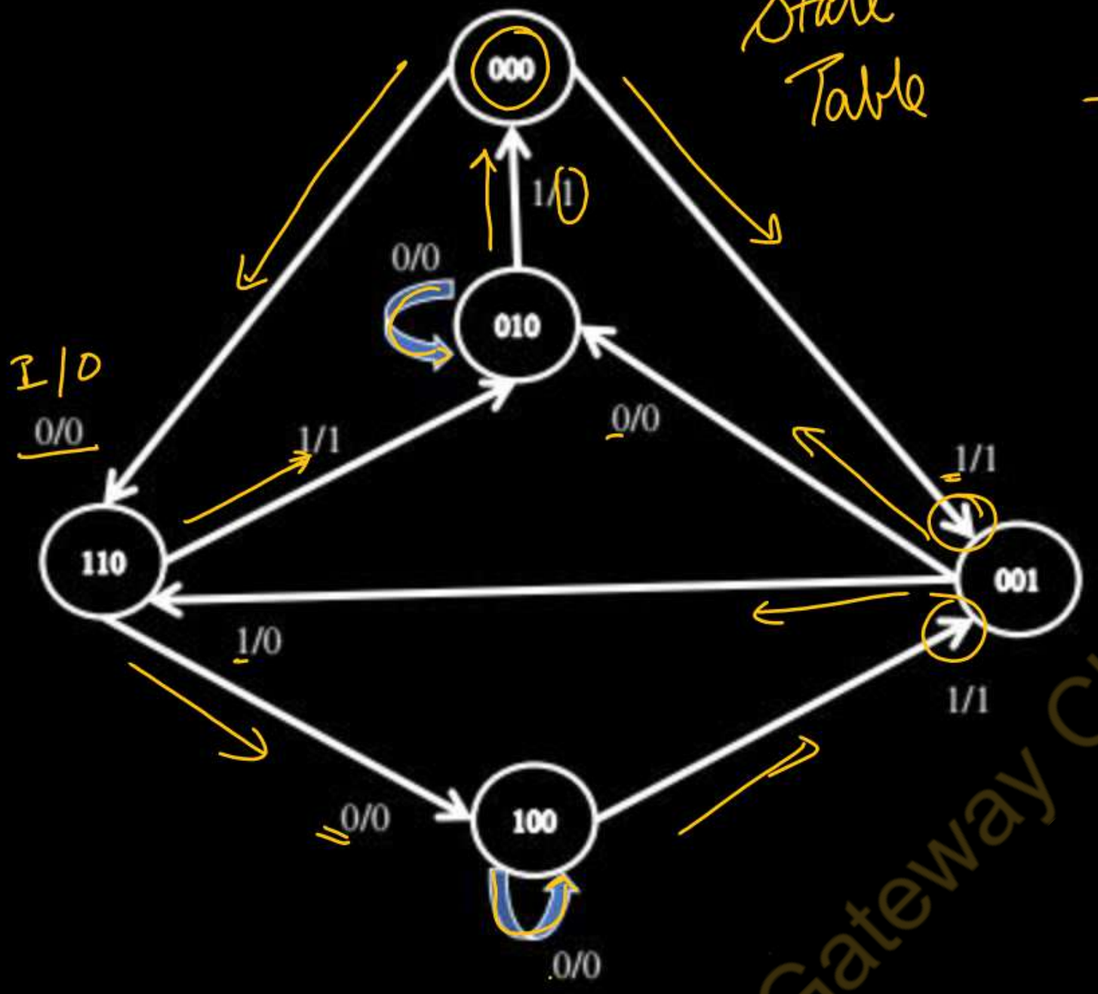
$D_A = A_n \bar{x} + B_n x$

$D_B = B_n \bar{x} + \bar{A}_n x$



Gateway Classes : 7455 9612 82

For the given state diagram, design the circuit using T Flip Flop (19-20)

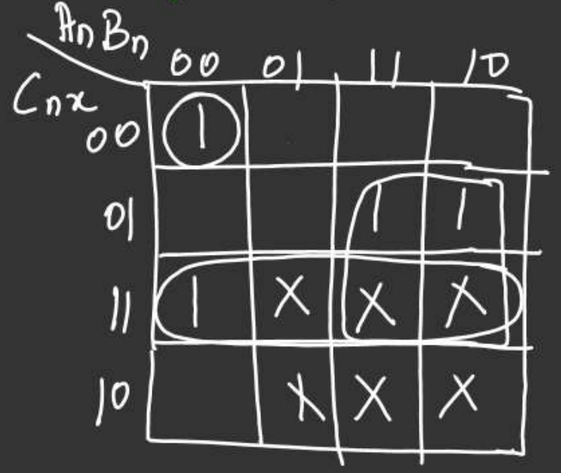


State Table

Present State A_n B_n C_n	I/p x	Next State A_{n+1} B_{n+1} C_{n+1}	O/p y	T_A	T_B	T_C
0 0 0	0	0 0 1	0	0	0	1
0 0 1	0	0 1 0	0	0	1	1
0 1 0	0	0 0 0	0	0	1	0
0 1 1	0	1 0 0	1	1	1	0
1 0 0	0	1 1 0	1	0	1	0
1 0 1	0	0 0 0	0	1	1	0
1 1 0	0	0 0 0	0	1	0	0
1 1 1	0	0 0 0	0	1	0	0
0 0 0	1	0 0 1	0	0	0	1
0 0 1	1	1 0 0	1	1	0	1
0 1 0	1	0 0 1	0	0	1	1
0 1 1	1	0 0 0	0	0	1	0
1 0 0	1	0 1 1	1	0	1	1
1 0 1	1	0 0 1	0	1	1	1
1 1 0	1	0 0 1	0	1	0	1
1 1 1	1	0 0 0	0	1	0	0

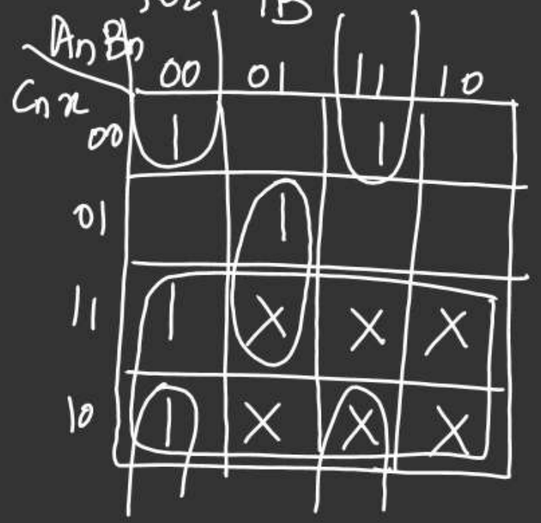
Gateway Classes : 7455 961284

for T_A



$$T_A = C_n x + A_n x + \bar{A}_n \bar{B}_n \bar{C}_n \bar{x}$$

for T_B

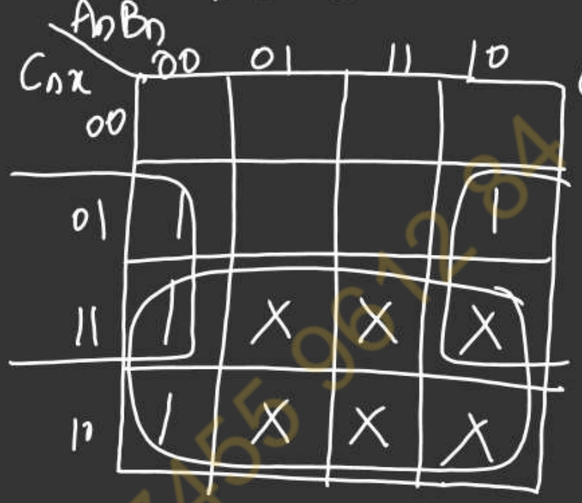


$$T_B = C_n + \bar{A}_n B_n + \bar{A}_n \bar{B}_n + A_n B_n$$

$$= C_n + \bar{A}_n [B_n + \bar{B}_n] + A_n B_n$$

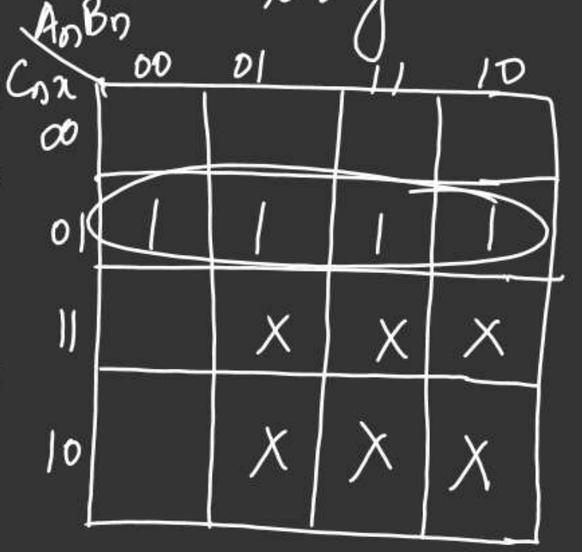
$$= C_n + \bar{A}_n + A_n B_n$$

for T_C



$$T_C = C_n + \bar{B}_n x$$

for y



$$y = \bar{C}_n x$$

Gateway Classes : 7465 06 12 34

State Equations

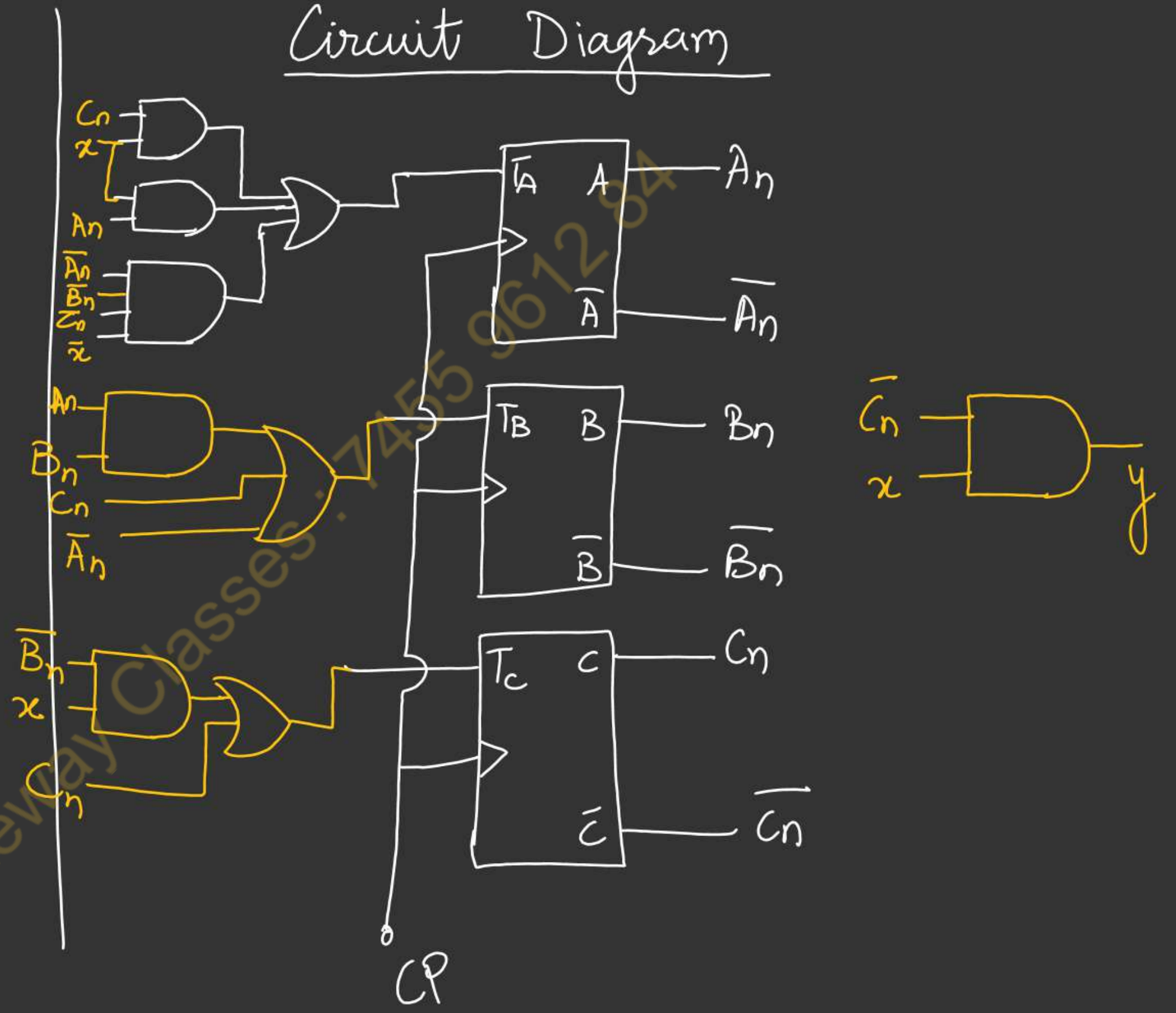
$$T_A = C_n x + A_n x + \bar{A}_n \bar{B}_n \bar{C}_n \bar{x}$$

$$T_B = C_n + \bar{A}_n + A_n B_n$$

$$T_C = C_n + \bar{B}_n x$$

$$y = \bar{C}_n x$$

Circuit Diagram



Gateway Classes: 7455 9612 84

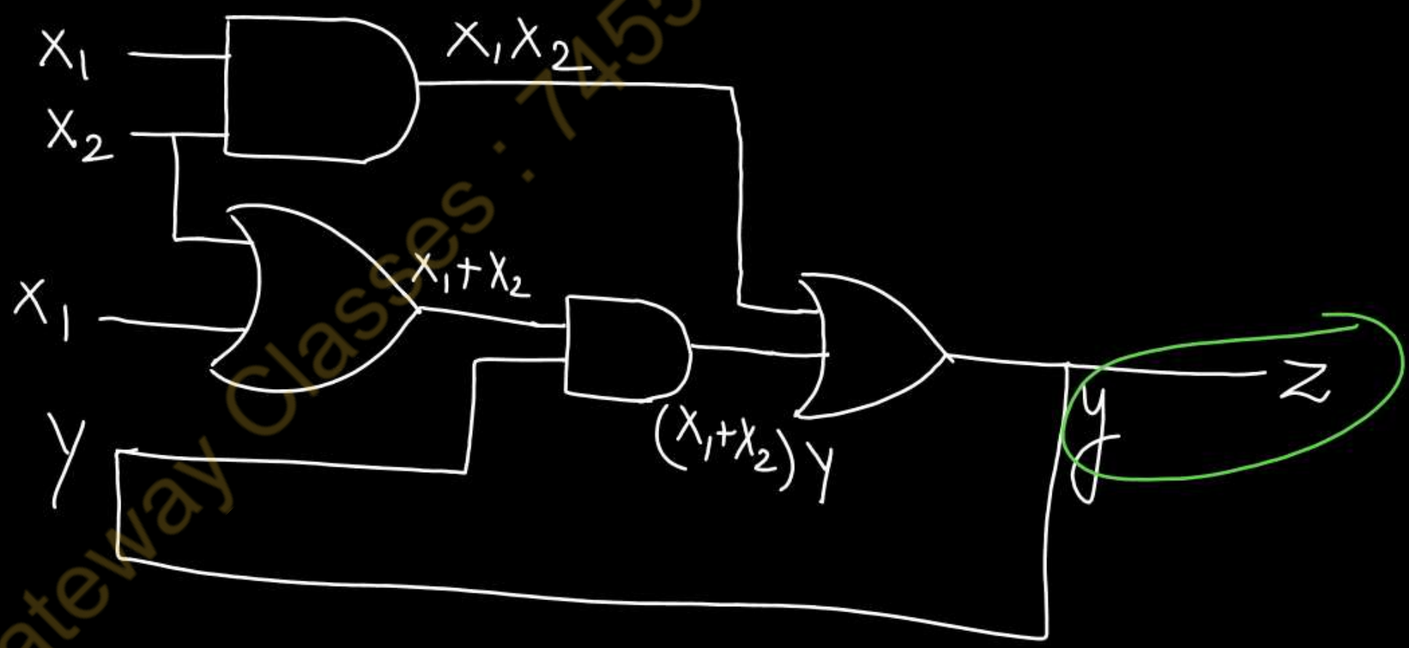
An asynchronous sequential logic circuit is described by the following excitation and output function $y = XIX2 + (X1 + X2)\,Y$ and output $Z = y$

(i) Draw the logic diagram of the circuit.

(ii) Derive the transition table and output map

(iii) Describe the behavior of the circuit. (18-19)

Logic Diagram:



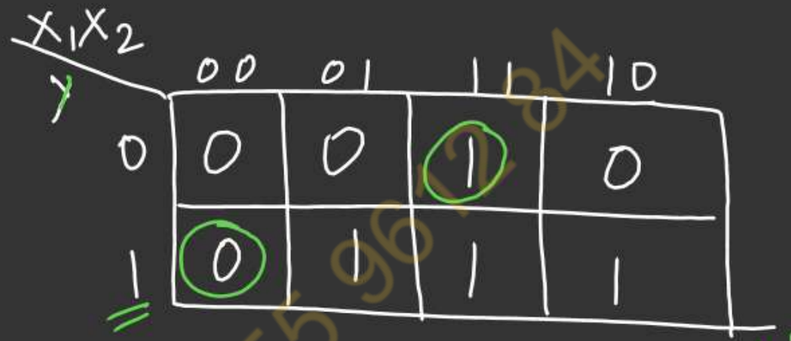
Gateway Classes : 7455 9612 84

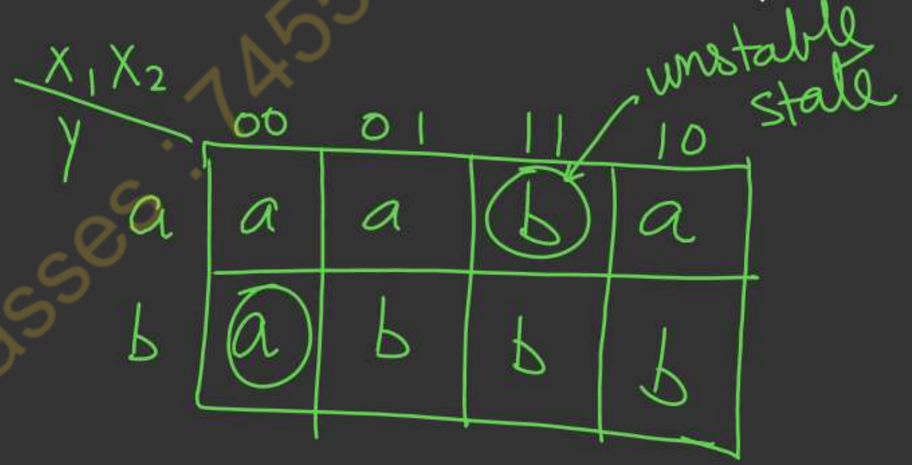
Transition Table

y	x_1	x_2	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$$y = x_1 x_2 + (x_1 + x_2)\, y$$

Output Map





Gateway Classes : 7455 96 12 84

DIGITAL SYSTEM DESIGN

UNIT 3 : Sequential logic design

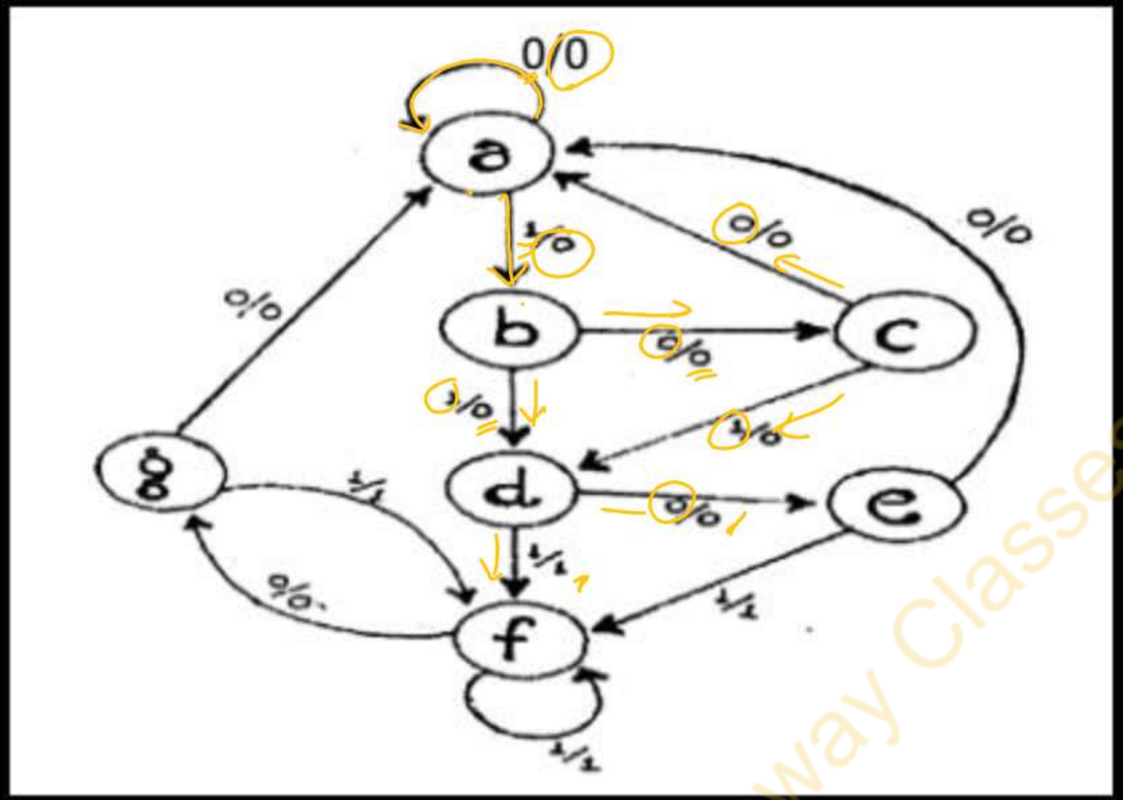
Lec 10

Gateway Classes : 7455 961284

Today's Target

- State Reduction
- Numerical Practice

Draw the reduced state' table and reduced state diagram for ;the siate table given below:



State Table

P. S.	N. S. x=0	N. S. x=1	O/P x=0	O/P x=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

Gateway Classes : 7455 9612 84

Reduced State Table

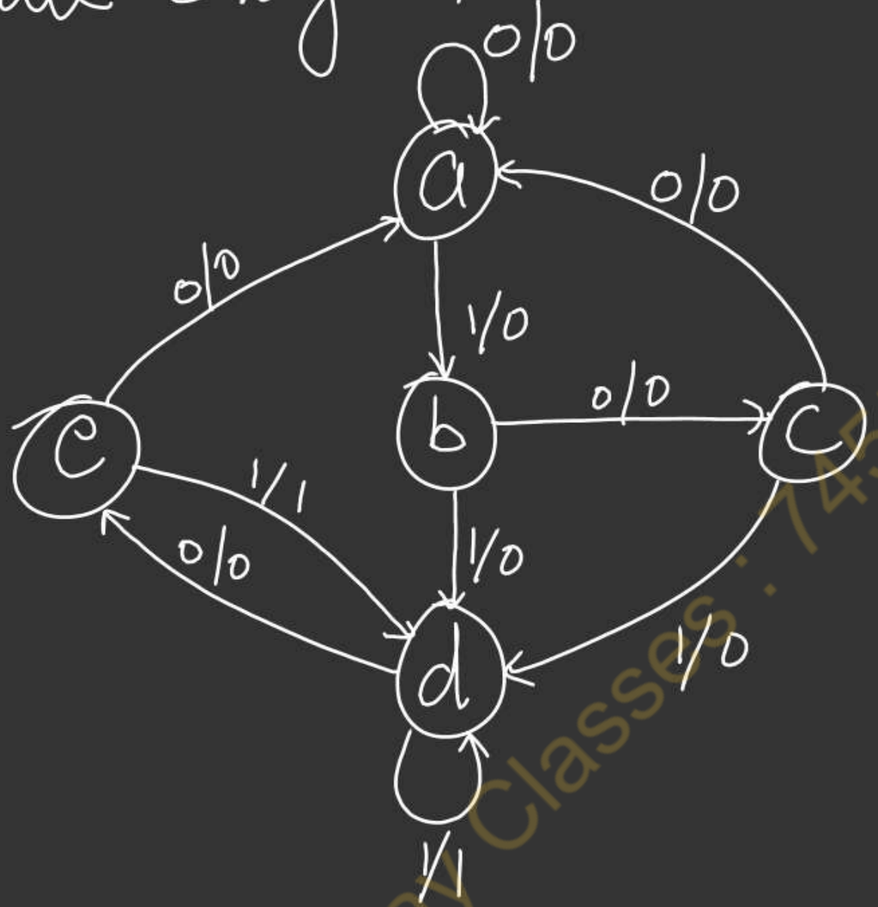
P.S.	N.S. $x=0$	N.S. $x=1$	O/P $x=0$	O/P $x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	~~g~~e	f	0	1

Reduced State Table

P.S.	N.S. $x=0$	N.S. $x=1$	O/P $x=0$	O/P $x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	~~f~~d	0	1
e	a	~~f~~d	0	1

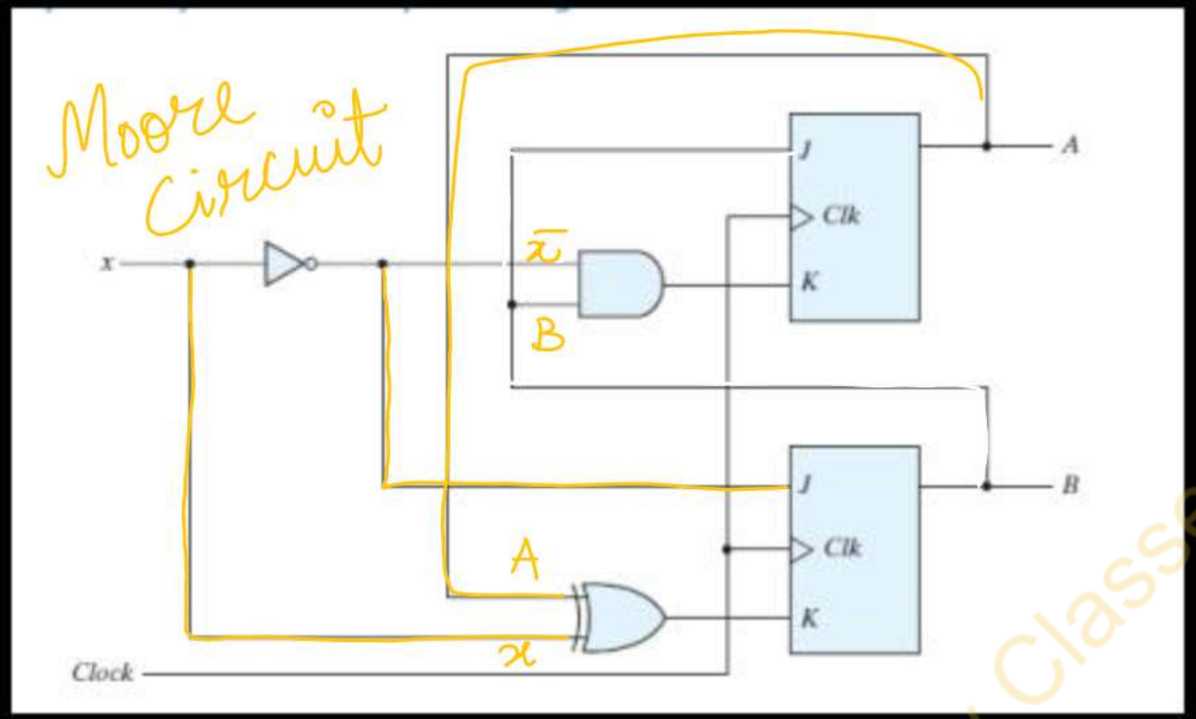
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State Diagram



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Derive the State Table, State equations and State Diagram for the given circuit:





State Equations:

$J_A = B$

$K_A = B\bar{x}$

$J_B = \bar{x}$

$K_B = A \oplus x$

State Table

P.S			N.S					
A	B	x	A_{n+1}	B_{n+1}	J_A	K_A	J_B	K_B

Gateway Classes: +91 55 9612 84

State Eq"

$J_A = B$

$K_A = B\bar{x}$

$J_B = \bar{x}$

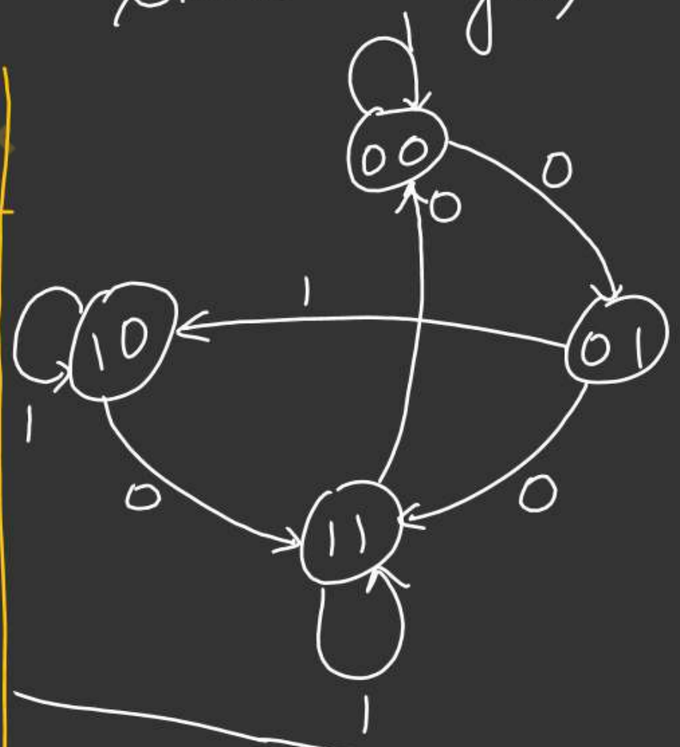
$K_B = A \oplus x$

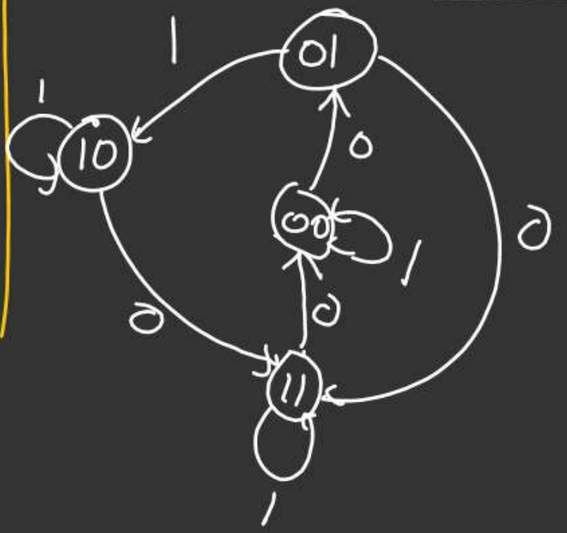
J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

State Table

P.S A	P.S B	i/p x	N.S. A_{n+1}	N.S. B_{n+1}	FF i/Ps J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

State Diagram





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Thank You