AKTU

GATEWAY CLASSES

Digital System Design

B.Tech. 3rd Sem

EC & Allied



Exam/Result Oriented Content

- ✓ Recorded Video Lectures
- ✓ Pdf Notes
- ✓ PYQs

DIGITAL SYSTEM DESIGN

UNIT 2 : Combinational circuits

Today's Target

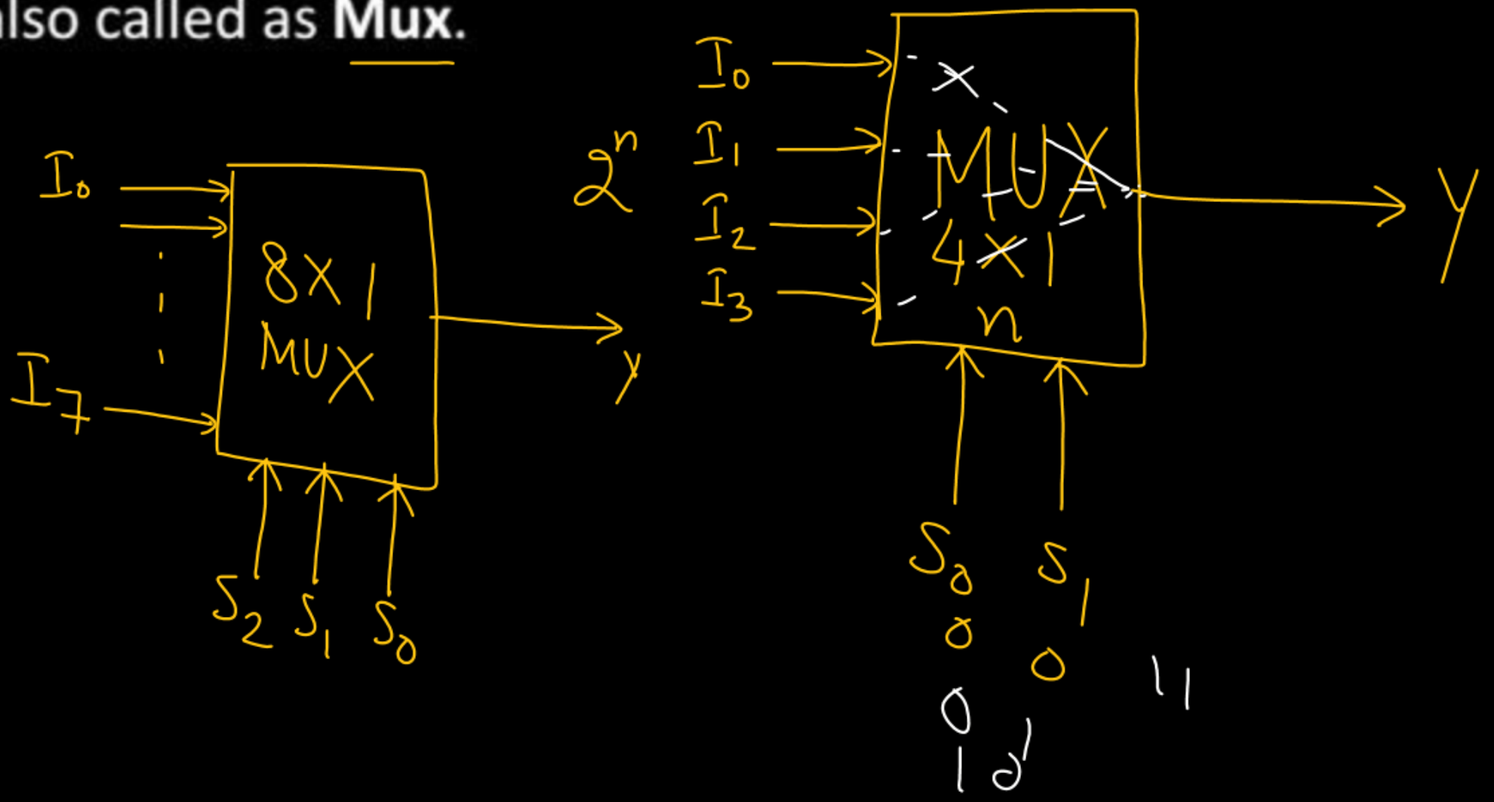
- MUX
- Implementation of Higher-order Multiplexers
- Numerical Practice of MUX
- DPP
- University Questions

UNIVERSITY QUESTIONS

YEAR	QUESTION	MARKS
22-23	Implement the function F = Σm(0,1,3,4,7,8,9,11,14,15) using 8:1 mux.	10 marks
20-21, 19-20	Implement a 4:1 multiplexer using 2:1 multiplexer.	2 marks
19-20	Implement a full adder by using 8:1 multiplexer.	10 marks
18-19	Implement the following Boolean function F (A, B, C, D) = (0, 1, 3, 4, 7, 8, 9, 11, 14,15) using (I) 4:1 MUX (ii) 2:1 MUX	10 marks

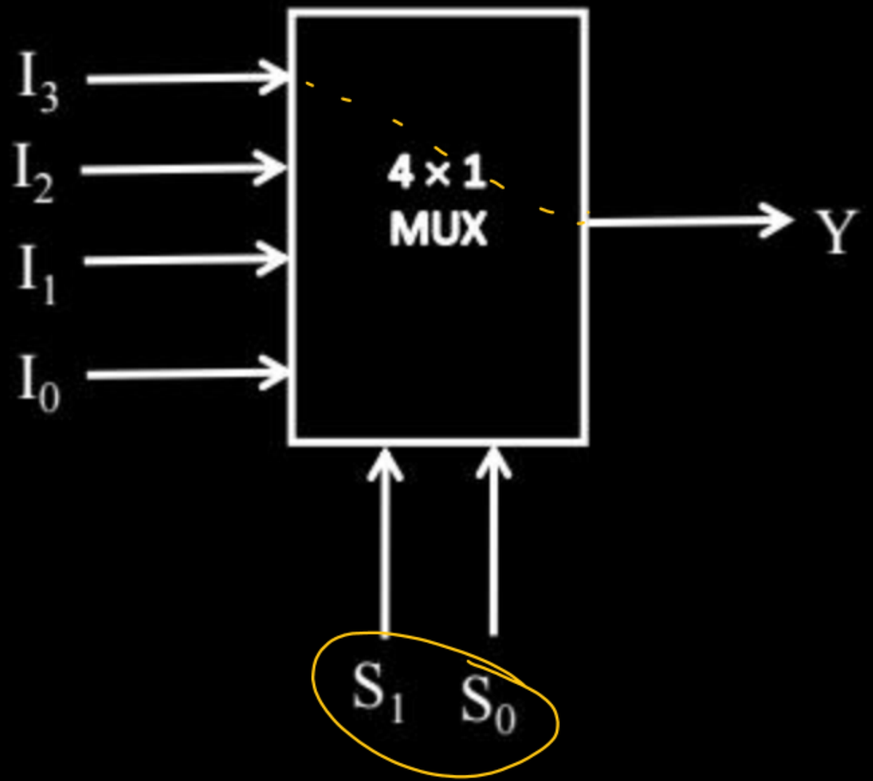
Multiplexers

- **Multiplexer** is a combinational circuit that has
- maximum of 2^n data inputs,
- 'n' selection lines and single output line.
- One of these data inputs will be connected to the output based on the values of selection lines.
- Multiplexer is also called as **Mux**.



4x1 Multiplexer

- four data inputs I_3, I_2, I_1 & I_0,
- two selection lines S_1 & S_0 and
- one output Y.
- The **block diagram** of 4x1 Multiplexer is shown in the following figure.



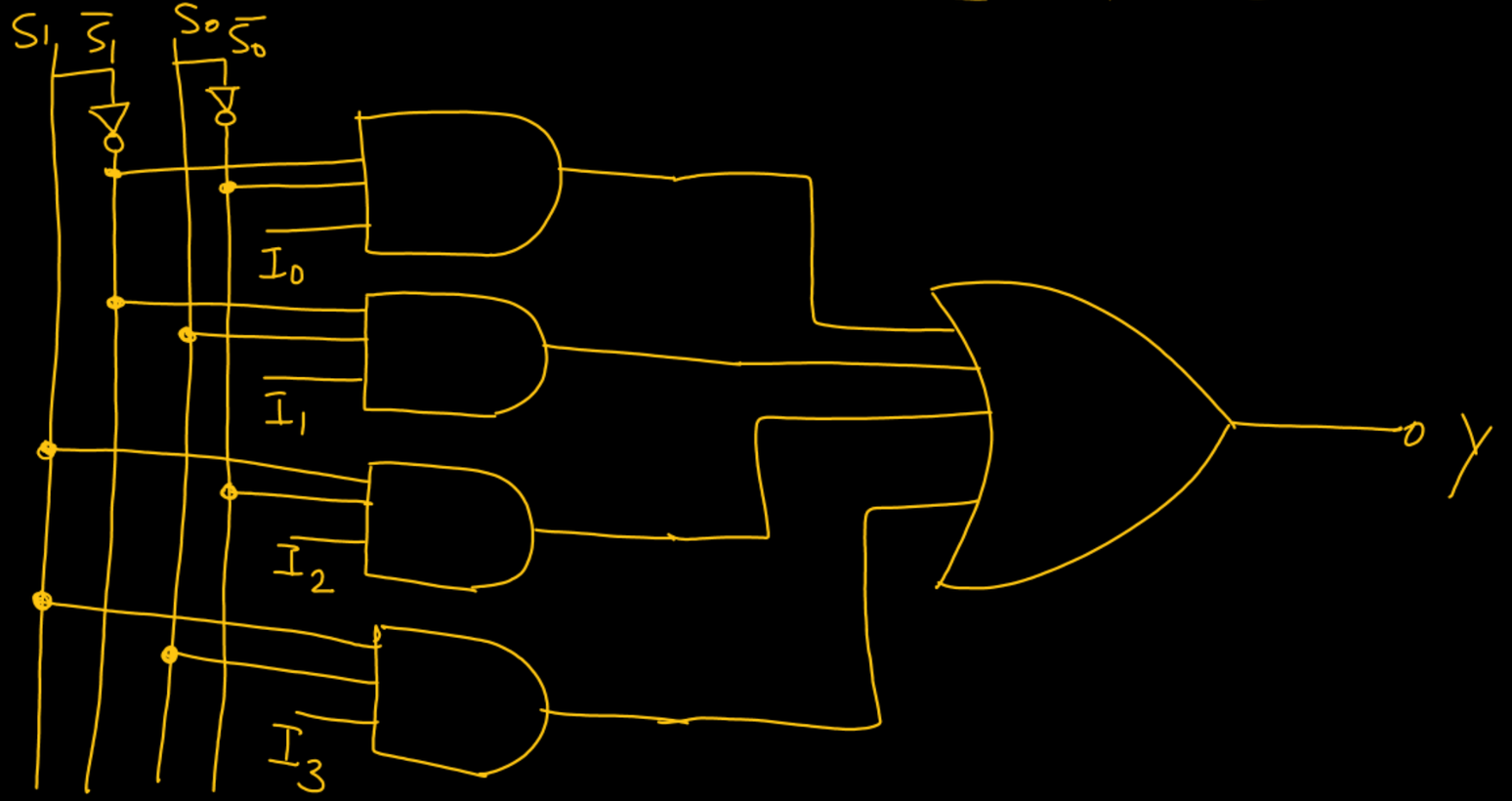
One of these 4 inputs will be connected to the output based on the combination of inputs present at these two selection lines.

Truth table of 4x1 Multiplexe

Selection Lines		Output
S1	S0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Boolean function for output :

$$Y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$

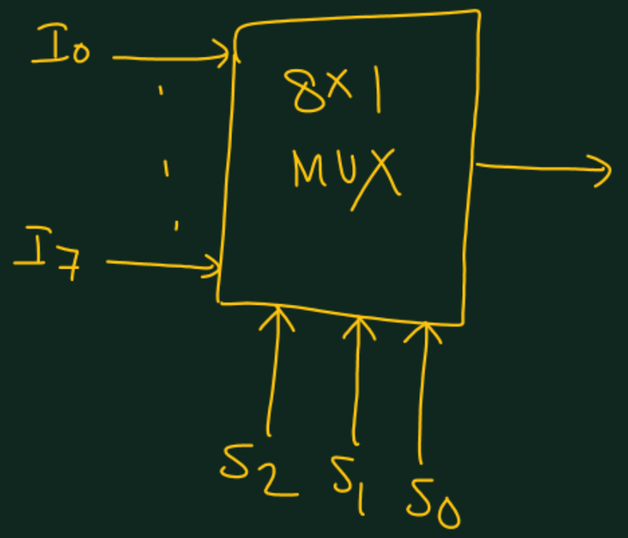


8 × 1 MUX

I/P = 8

Select = 3

O/P = 1



S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

$$Y = \bar{S}_2 \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_2 \bar{S}_1 S_0 I_1 + \bar{S}_2 S_1 \bar{S}_0 I_2 + \bar{S}_2 S_1 S_0 I_3 + S_2 \bar{S}_1 \bar{S}_0 I_4 + S_2 \bar{S}_1 S_0 I_5 + S_2 S_1 \bar{S}_0 I_6 + S_2 S_1 S_0 I_7$$

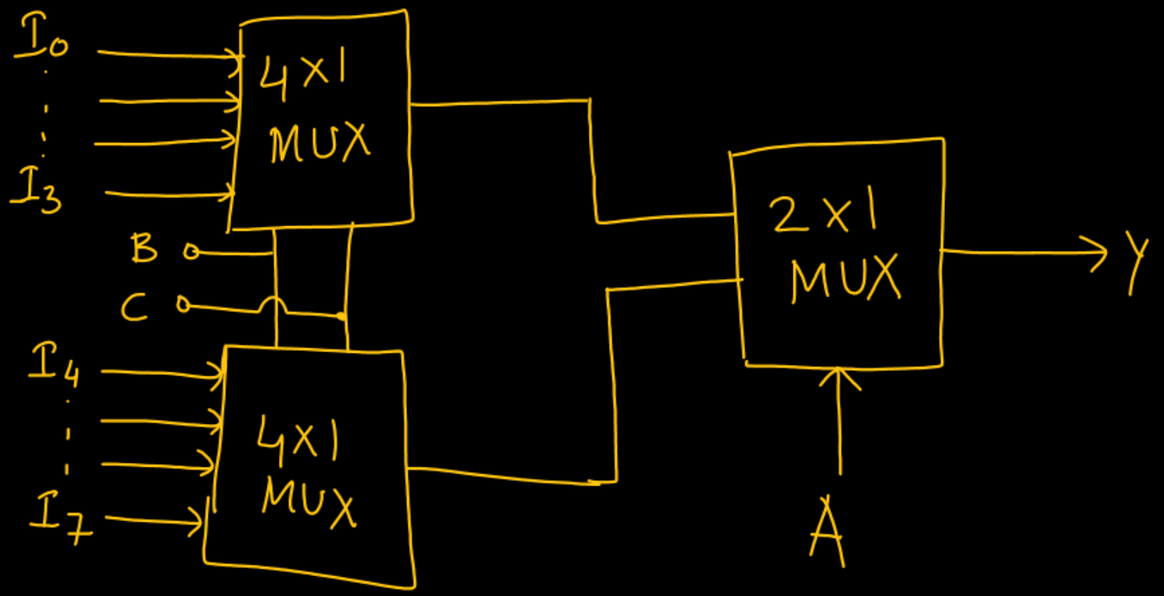
Implementation of Higher-order Multiplexers.

- 8x1 Multiplexer using 4x1 Multiplexers and 2x1 Multiplexer.

$$\text{No. of MUX Req.} = \frac{8 \times 1}{4 \times 1} = 2$$

8x1 : $n = 3$ A (B C)

4x1 : $n = 2$



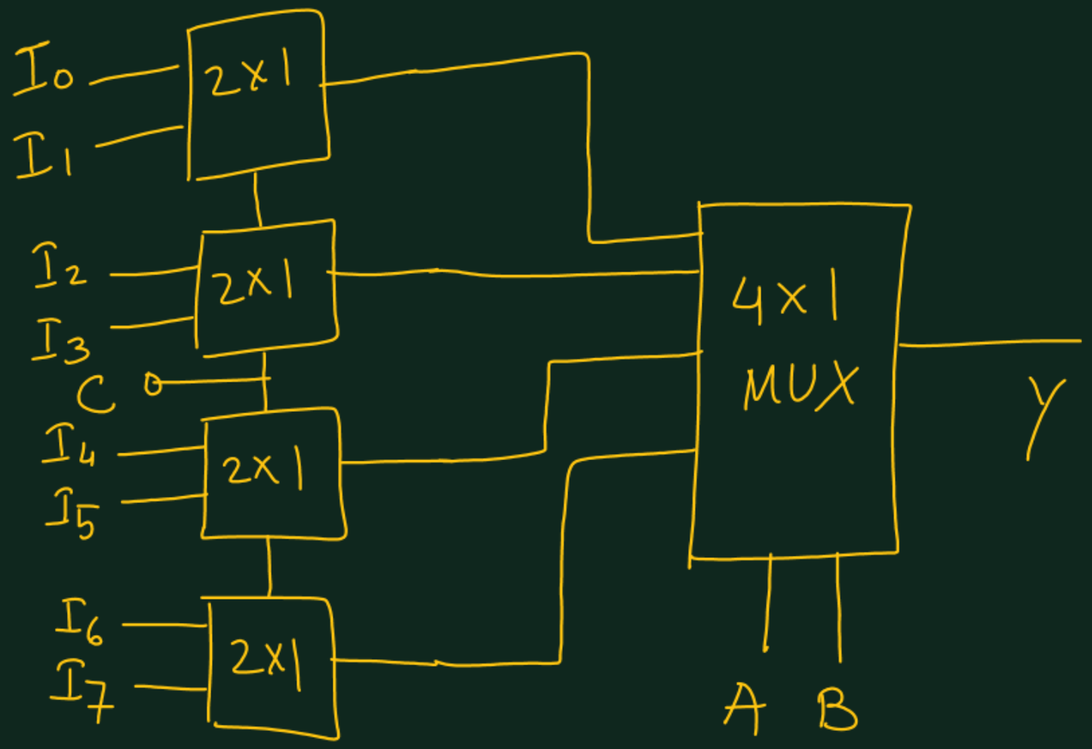
8×1 MUX using 2×1 MUX & 4×1 MUX

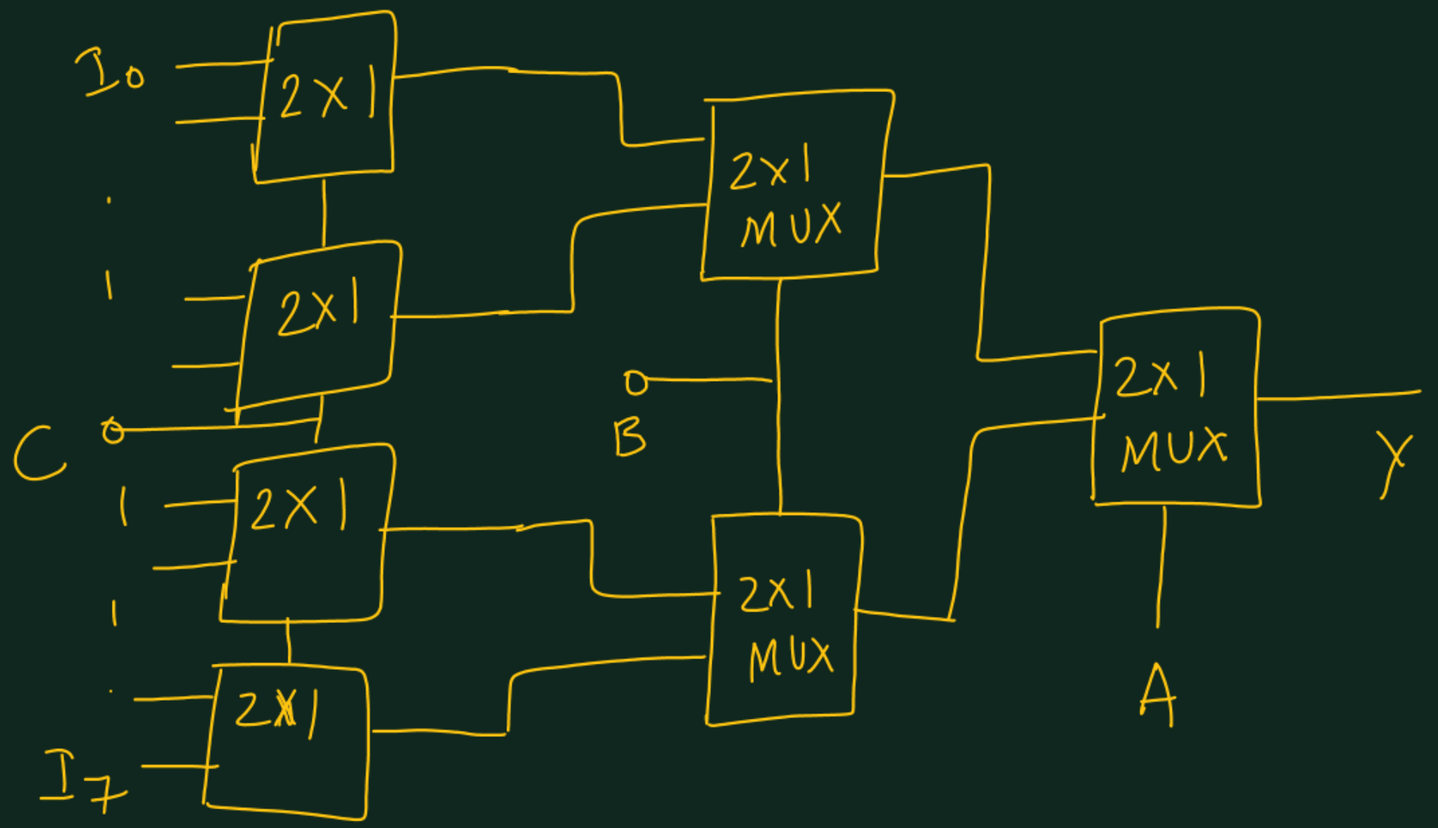
$$\text{no. of req. MUX} = \frac{8\times1}{2\times1} = 4$$

A B C

8×1 : n = 3

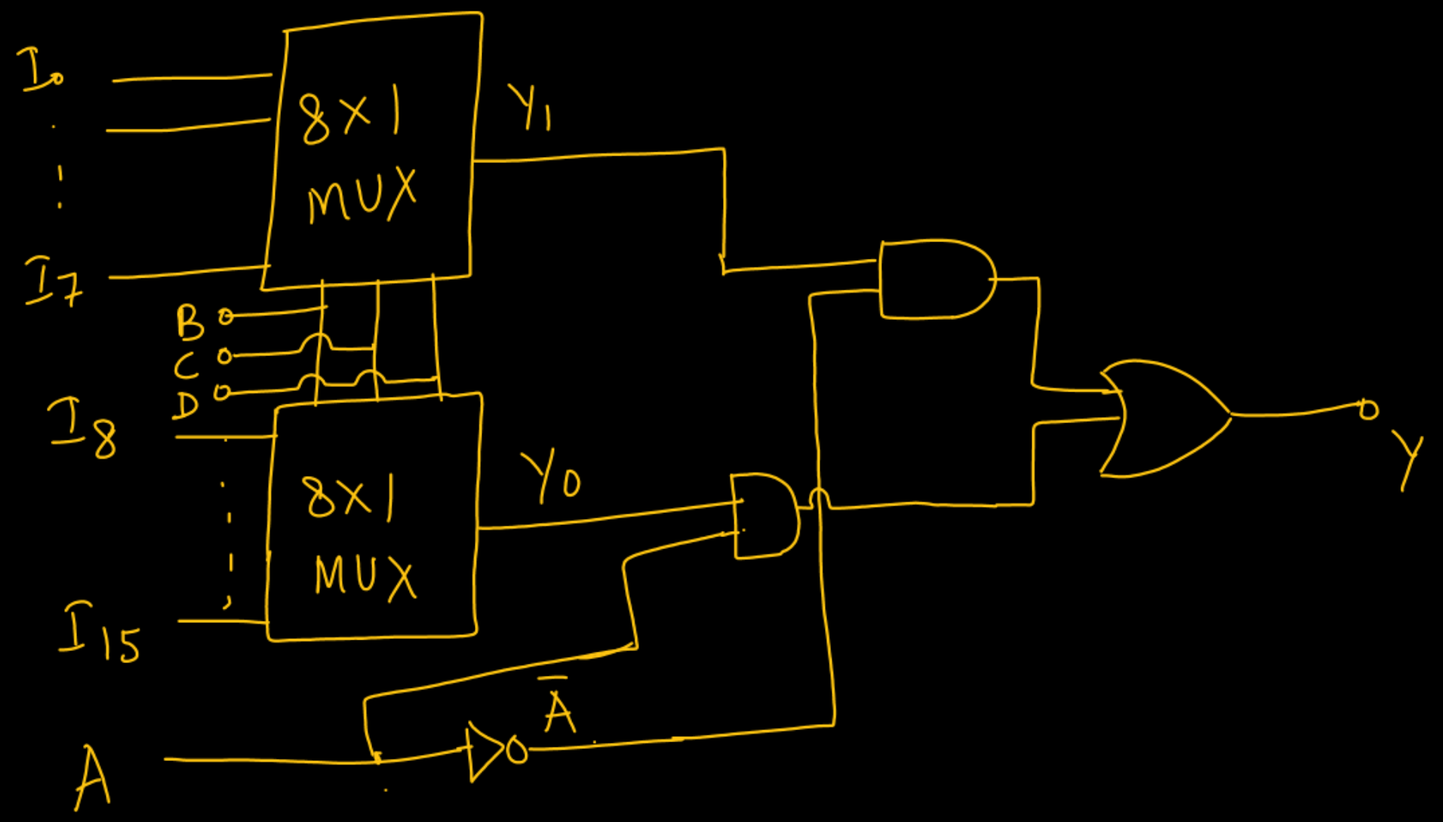
2×1 : n = 1





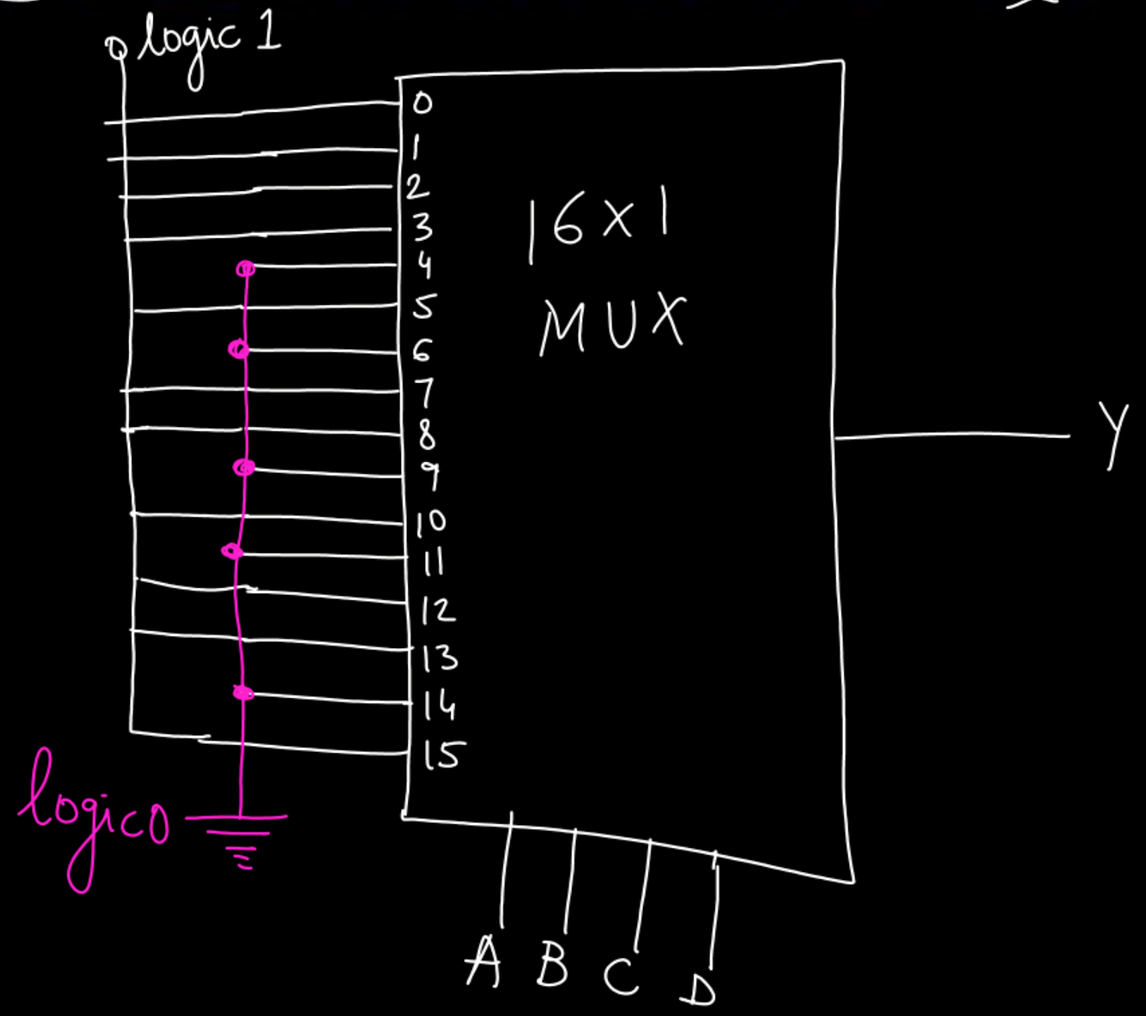
ABC

16x1 Multiplexer using 8x1

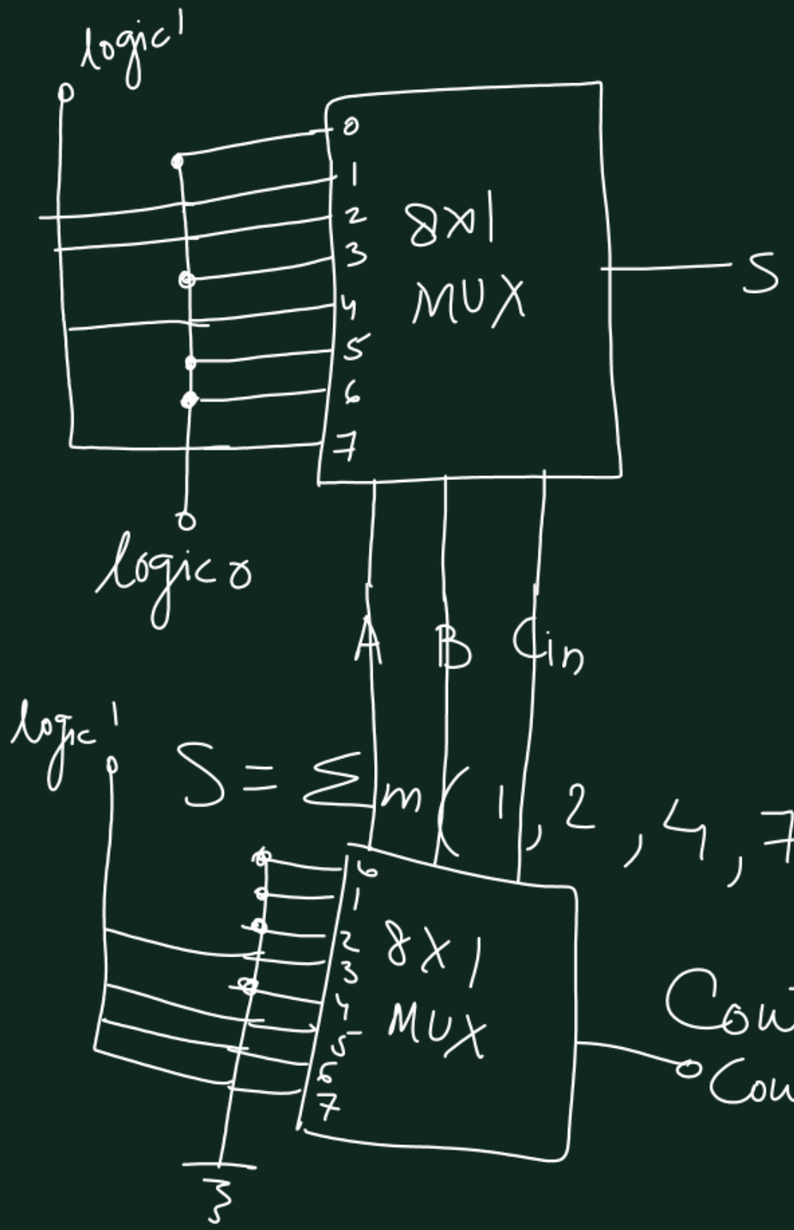


Design multiplexer implementations for the following functions using the numerical method.

- Z= F(A,B,C,D) = ∑m(0,1,2,3,5,7,8,10,12,13,15)



Full Adder

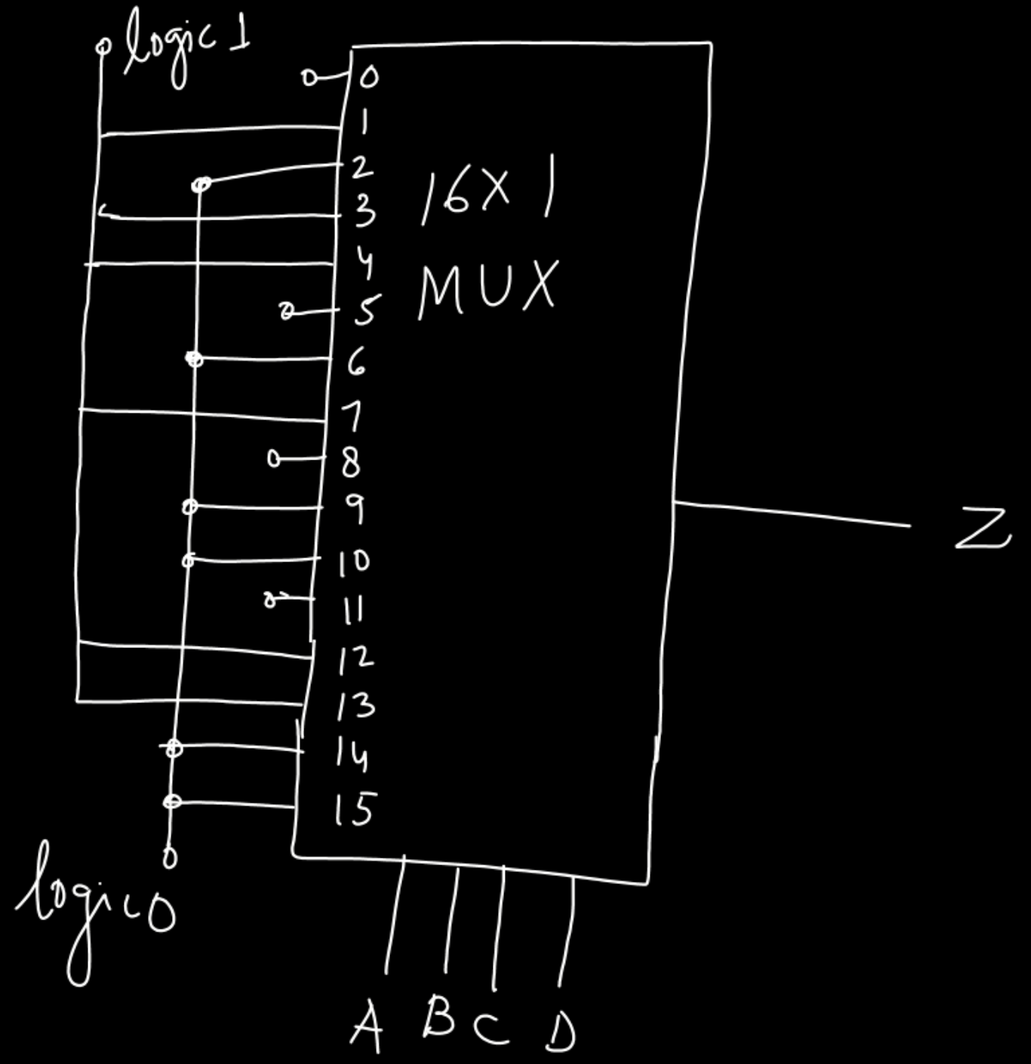


A	B	Cin	S	Cout
0	0	0	0	
0	0	1	1	
0	1	0	1	
0	1	1	0	1
1	0	0	1	
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$S = \Sigma m(1, 2, 4, 7)$

$Cout = \Sigma m(3, 5, 6, 7)$

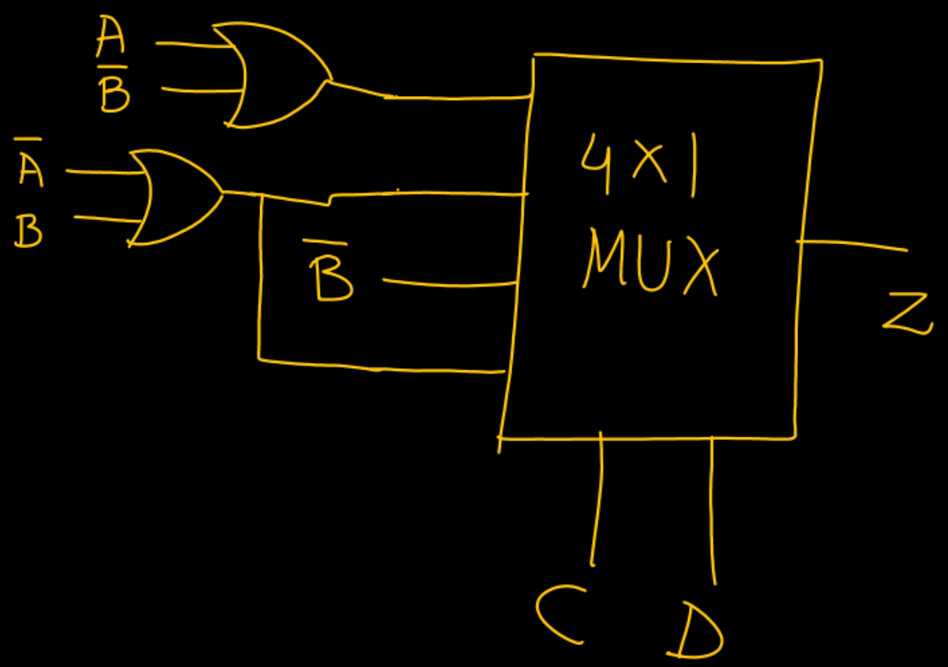
$$Z = F(A,B,C,D) = \sum m(1,3,4,7,12,13) + d(0,5,8,11)$$



Implement Z= F(A,B,C,D) = ∑m(0,1,2,3,5,7,8,10,12,13,15) using 8×1 MUX

$\bar{A}$	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15

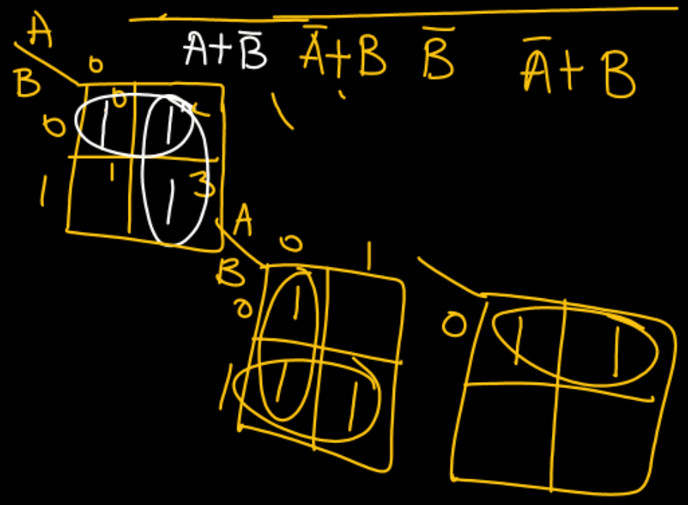
1	$\bar{A}$	1	$\bar{A}$	A	1	0	1	

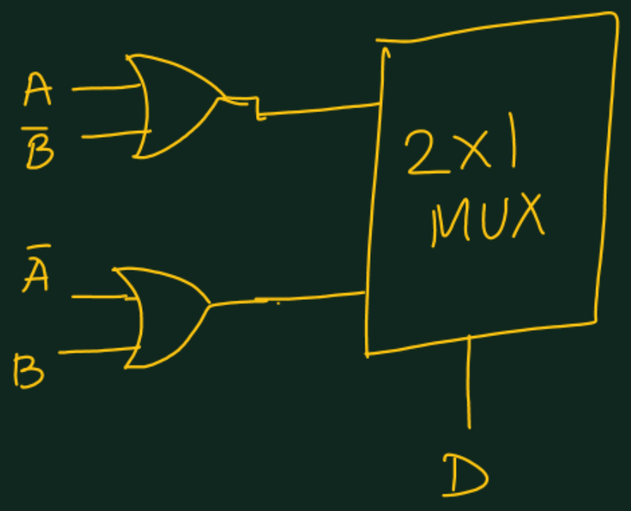




$\bar{A}\bar{B}$	0	1	2	3
$\bar{A}B$	4	5	6	7
$A\bar{B}$	8	9	10	11
AB	12	13	14	15

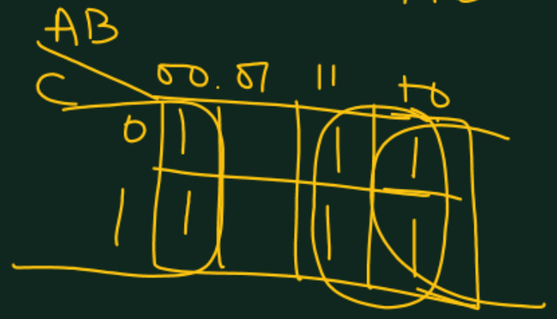
$A+\bar{B}$	$\bar{A}+B$	$\bar{B}$	$\bar{A}+B$	

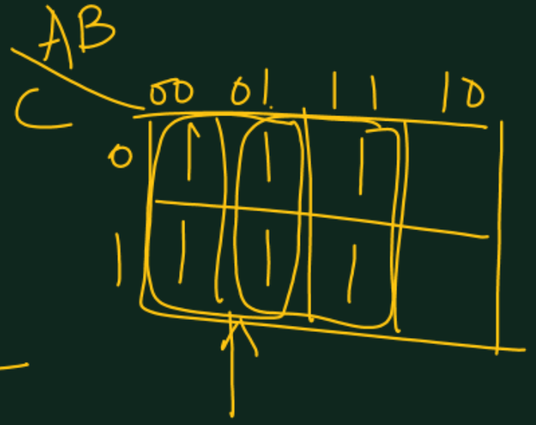




	$\bar{D}$	D
$\bar{A}\bar{B}\bar{C}$	0	1
$\bar{A}\bar{B}C$	2	3
$\bar{A}B\bar{C}$	4	5
$\bar{A}BC$	6	7
$A\bar{B}\bar{C}$	8	9
$A\bar{B}C$	10	11
$AB\bar{C}$	12	13
ABC	14	15

$\bar{A}+\bar{B}$ $\bar{A}+B$





DPP

a) Design a 16 × 1 MUX using basic logic gates.

b) Z= F(A,B,C,D) = A'C'D' + BC'D' + AB'C' + A'BC'D + A'B'CD' using 16 × 1 MUX and 8 × 1 MUX

$$= \bar{A}(B+\bar{B})\bar{C}\bar{D}$$

$$= \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D}$$

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Thank You

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