AKTU

GATEWAY CLASSES

Digital System Design

B.Tech. 3rd Sem

EC & Allied



Exam/Result Oriented Content

- ✓ Recorded Video Lectures
- ✓ Pdf Notes
- ✓ PYQs

DIGITAL SYSTEM DESIGN

UNIT 4 : Logic families and semiconductor memories

Lec 2

Today's Target

- Transistor-transistor logic (TTL)
- TTL NAND Gate
- **TTL NAND gate with open collector output**
- University Questions

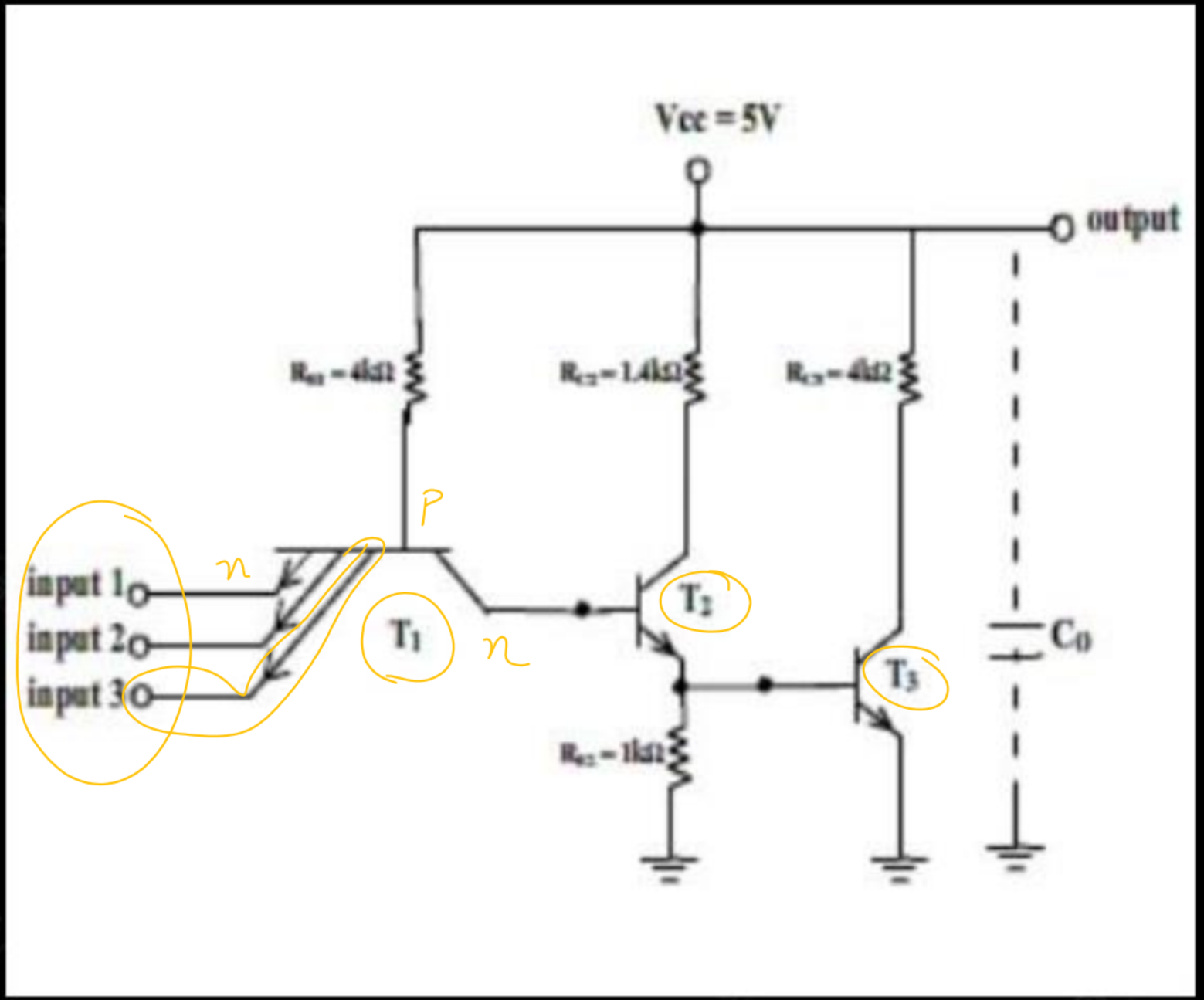
UNIVERSITY QUESTIONS

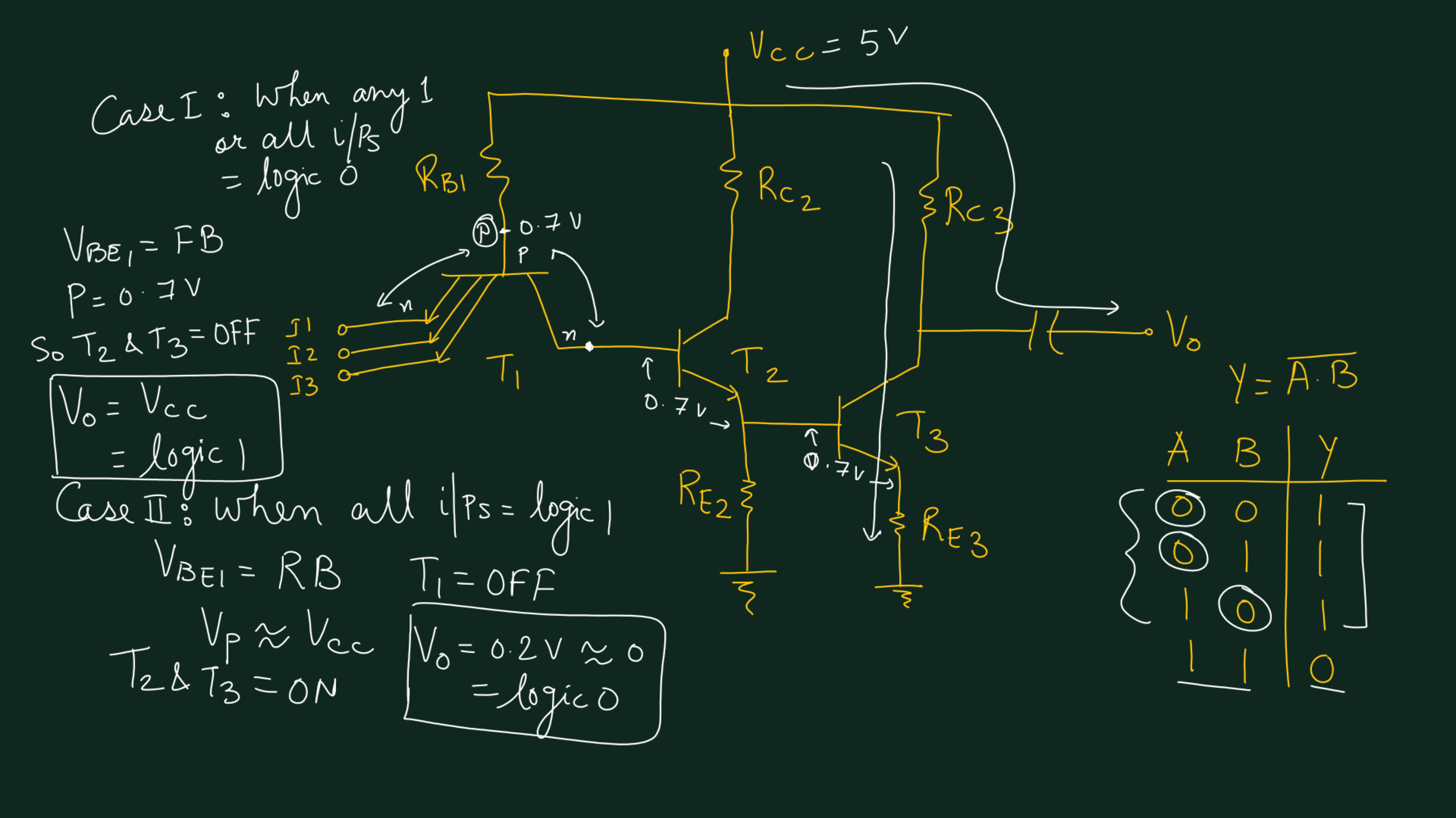
YEAR	QUESTIONS	MARKS
21-22	What do you understand by digital TTL?	2 Marks
21-22 20-21	With the help of a neat diagram, explain the working of a two-input TTL NAND gate.	10 Marks
19-20	Draw three input standard TTL NAND gate circuit and explain its operation.	10 Marks

Transistor-transistor logic (TTL)

- based on bipolar transistors one of the most widely used families of small- and medium-scale devices
- rarely used for VLSI
- typically operated from a 5V supply
- typical noise immunity about 1 – 1.6 V
- many forms, some optimised for speed, power, etc.
- High-speed versions comparable to CMOS (~ 1.5 ns)
- low-power versions down to about 1 mW/gate

TTL NAND Gate

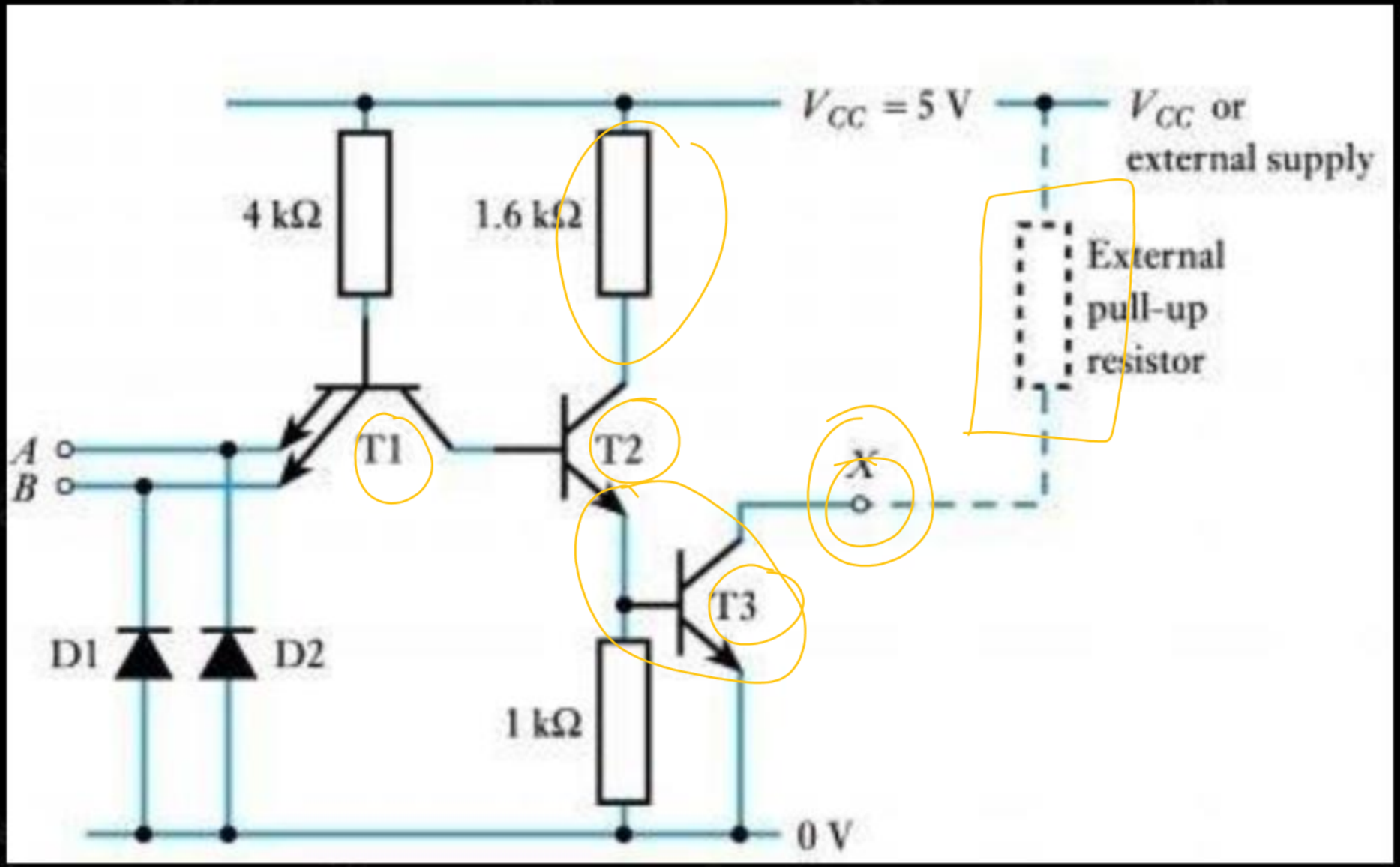



Case I : When any 1 or all i/Ps = logic 0
V_{BE_1} = FB
P = 0.7 V
So T_2 & T_3 = OFF
V_o = V_{cc} = logic 1
Case II : When all i/Ps = logic 1
V_{BE1} = RB
T_1 = OFF
$V_P \approx V_{cc}$
T_2 & T_3 = ON
V_o = 0.2 V ≈ 0 = logic 0
V_{cc} = 5 V
R_{B1}
R_{C2}
R_{C3}
R_{E2}
R_{E3}
T_1
T_2
T_3
P
n
I1
I2
I3
0.7 V
V_o
$Y = \overline{A \cdot B}$
A B Y
0 0 1
0 1 1
1 0 1
1 1 0

TTL NAND Gate:

- Input terminals: The emitter of Q1 Output terminals: collector of Q2
- When any input = logic '0'
- Q1 emitter junction is forward biased. Also, its collector junction is FB,
- so Q1 goes in saturation.
- Base of Q2 is at Low voltage
- This causes base-emitter junction of Q2 to be RB, so Q2 goes in cut-off
- Hence output is 5V or logic '1'
- When all inputs = logic '1'
- Q1 emitter junction is RB. so Q1 goes in cut-off.
- Its collector voltage increases This forward biases Q2,
- so Q2 goes into saturation
- Hence output is 0V

A TTL NAND gate with open collector output



A TTL NAND gate with open collector output:

- Its similar to the previous circuit.
- Q2 is used as an emitter follower.
- The output of Q2 is fed to the input of Q3.
- Collector of Q2 and Q3 are in phase.
- This circuit needs an external 'Pull- up' resistor between output and power supply.
- The disadvantage of open- collector gate is their slow switching speed.
- The pull-up resistance is few kilo ohms. Gives a relatively long time constant, when multiplied by the stray output capacitance.
- Is worst when output goes from low to high.
- Open collector circuits are used to interface different families of devices that have different operating voltage levels.
- The open-collector transistor can be rated to withstand a higher voltage than the chip supply voltage.

Applications of open-collector output:

It is used in 3 major applications:

- In driving lamps or relays
- In performing wired logic
- In the construction of a common bus system

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Thank You